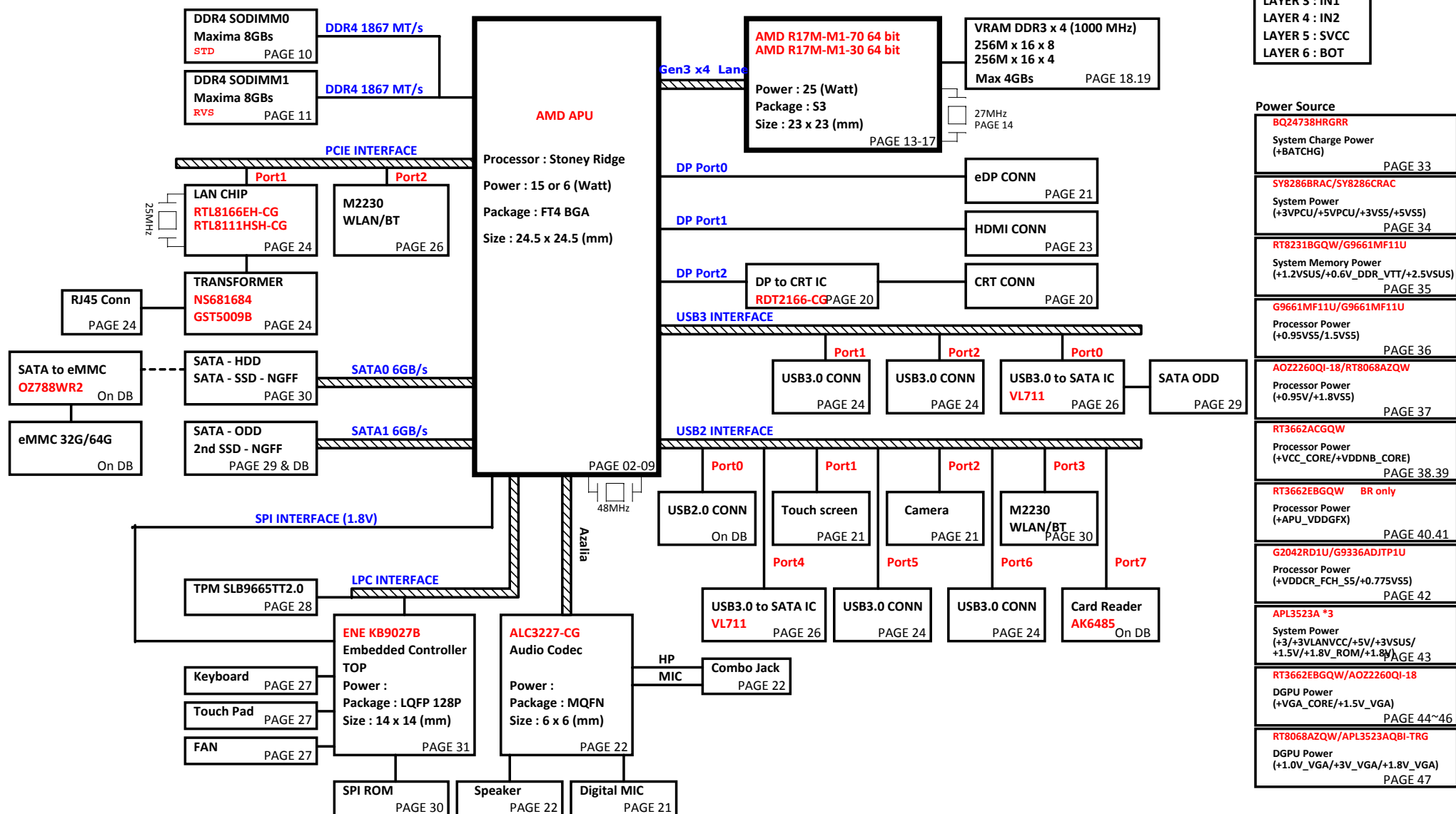
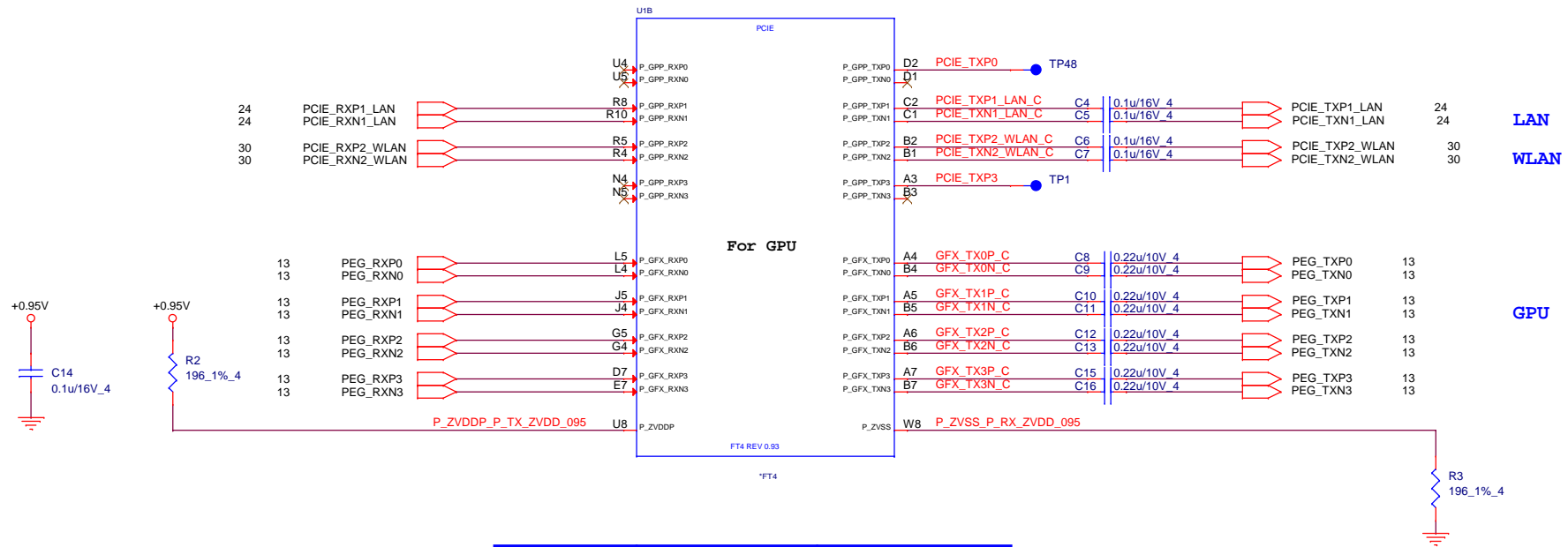


# NFL-C 14" AMD SR FT4 DIS/UMA Block Diagram



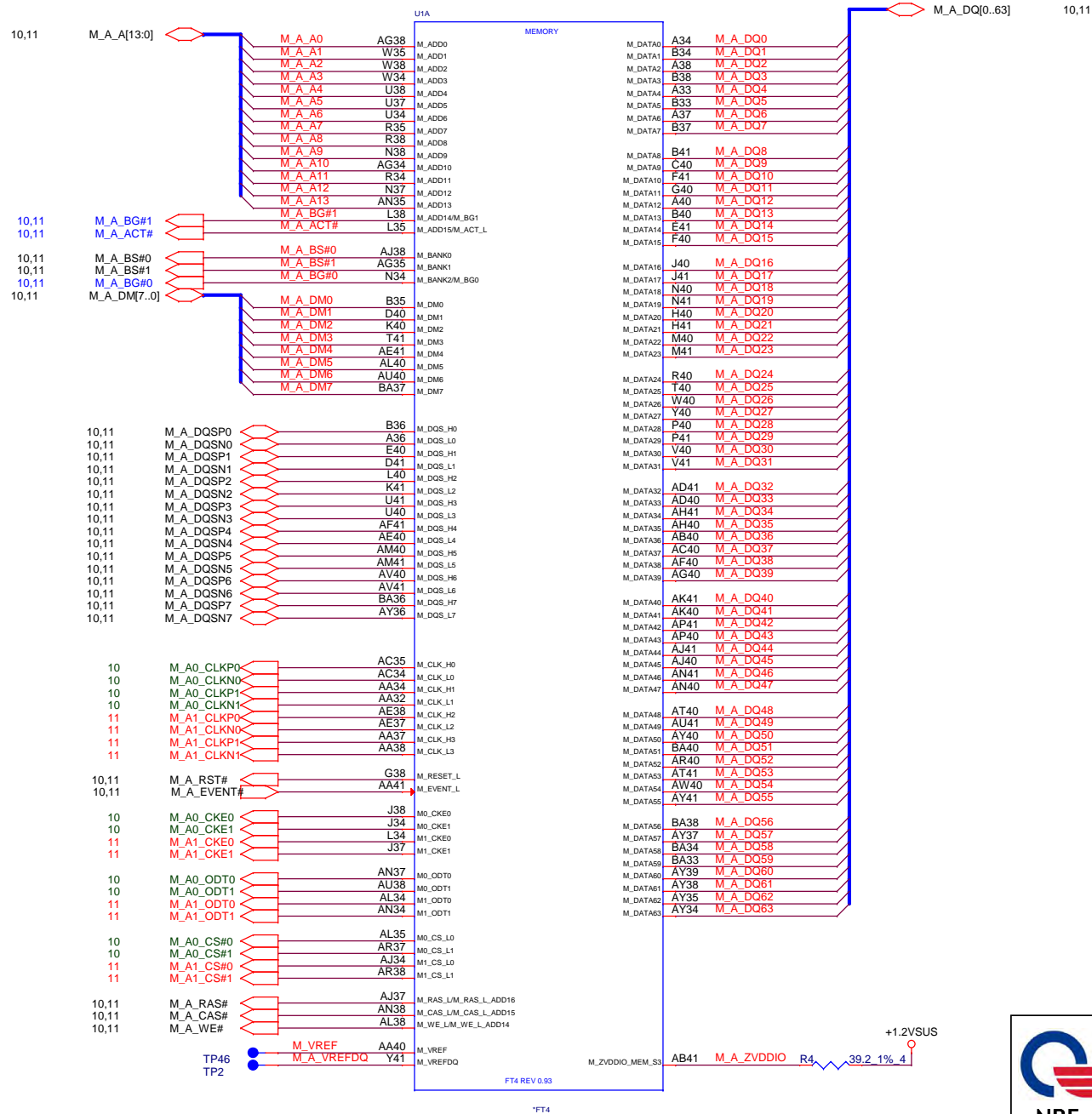



	QBCON PN	TOP BSQ
A9-9420	AJ094208T02	AJ094208T01
A6-9220	AJ09220RT01	AJ09220RT00
A4-9120	AJ09120UT01	AJ09120UT00
A6-9200e	AJ00920UT01	AJ00920UT00
E2-9000e	AJ900EAVT01	AJ900EAVT00



**PROJECT : Rams 0P2/0P2A**  
Quanta Computer Inc.

Size	Document Number	Rev
	ST 17(PCIE)	1A
Date: Wednesday, March 08, 2017	Sheet 2 of 48	

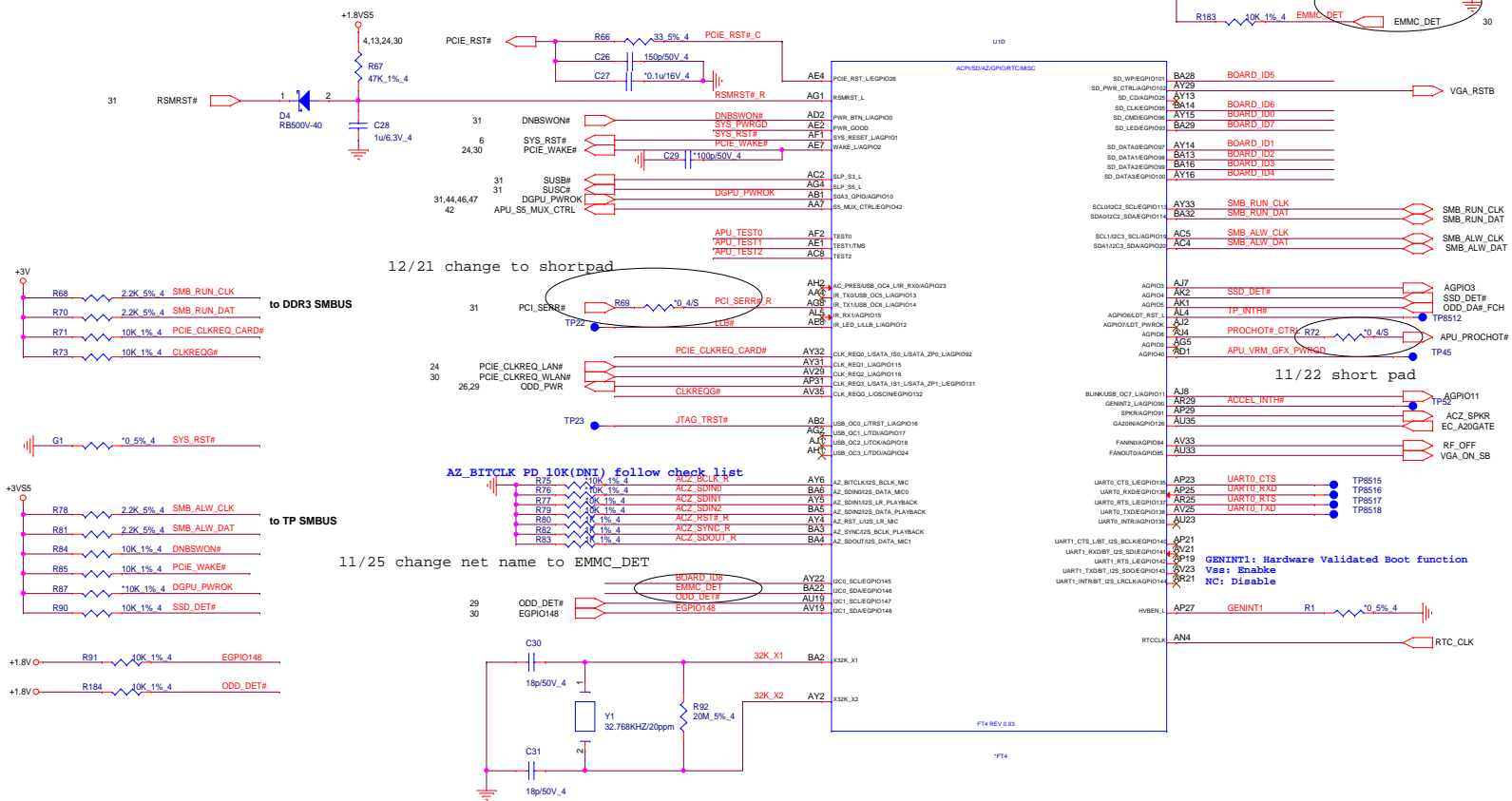




**PROJECT : Rams OP2/OP2A**  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>ST 277(MEM)</b>	1A
Date: Wednesday, March 08, 2017		
Sheet 3 of 48		





Board ID [0]	Definition
0	UMA
1	DIS

Board ID [2:1]	Definition
00	14"
01	Reserve
10	Reserve
11	Reserve

Board ID [4:3]	Definition
00	Reserve
01	Reserve
10	Reserve
11	Reserve

Board ID [5]	Definition
0	BR
1	SR

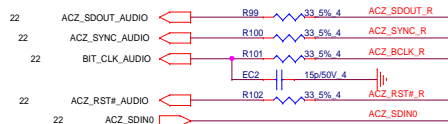
Board ID [6]	Definition
0	VRAM x8
1	VRAM x4

Board ID [7]	Definition
0	R17M-M1-70
1	R17M-M1-30

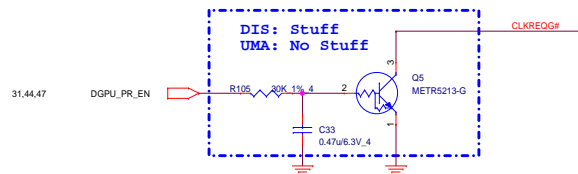
Board ID [8]	Definition
0	6W CPU
1	15W CPU

12/21 add CPU Watt.

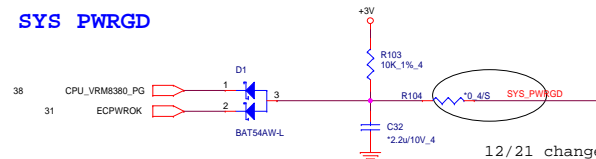
## HDA INTERFACE



## GPU CLK REQ

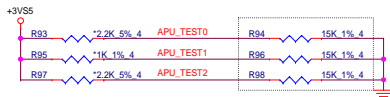


## SYS PWRGD



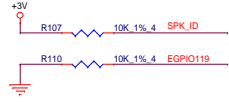
12/21 change to shortpa

Follow AMD checklist 55347 suggestion.



TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAP pins are overloaded for multiple functions, in this configuration the FCH JTAP are used as non-JTAP pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAP multi-function pins are configured as JTAP pins, in this configuration the FCH TAP can be accessed from FCH JTAP pins
1	TMS	1	Use on ATE only Yuba JTAP enabled

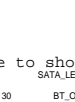
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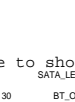
12/21 change to shortpad

HDD

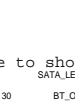
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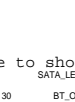
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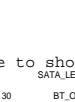
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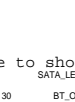
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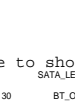
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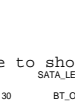
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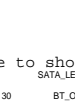
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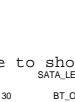
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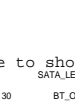
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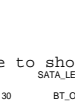
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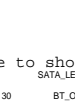
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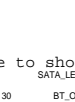
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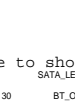
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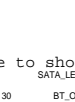
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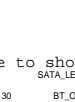
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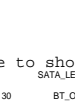
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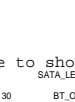
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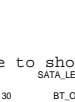
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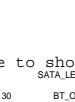
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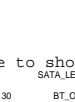
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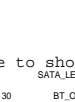
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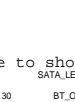
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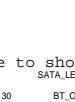
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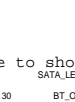
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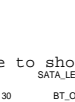
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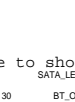
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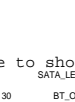
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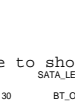
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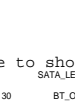
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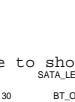
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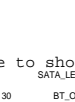
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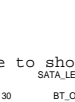
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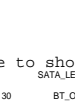
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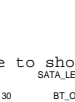
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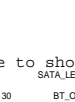
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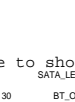
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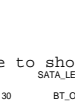
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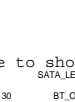
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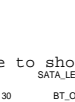
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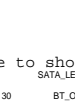
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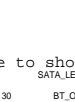
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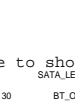
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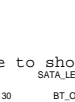
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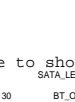
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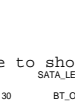
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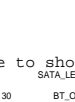
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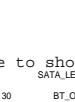
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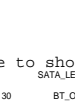
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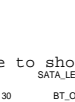
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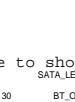
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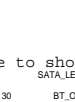
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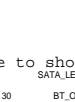
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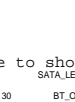
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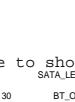
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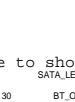
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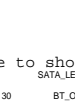
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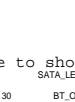
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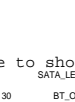
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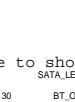
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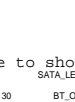
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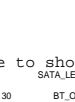
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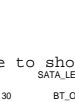
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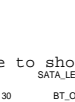
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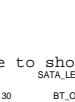
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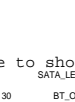
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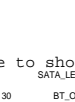
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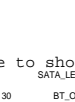
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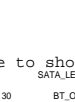
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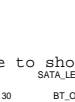
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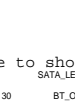
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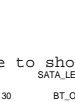
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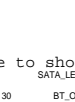
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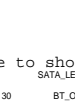
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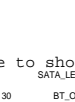
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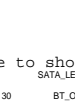
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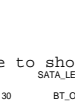
## Follow Checklist



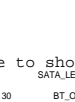
## Follow Checklist



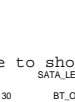
## Follow Checklist



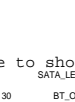
## Follow Checklist



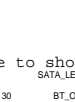
## Follow Checklist



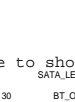
## Follow Checklist



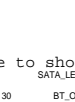
## Follow Checklist



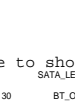
## Follow Checklist



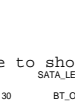
## Follow Checklist



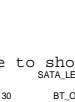
## Follow Checklist



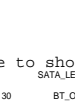
## Follow Checklist



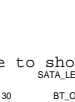
## Follow Checklist



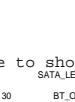
## Follow Checklist



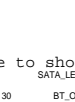
## Follow Checklist



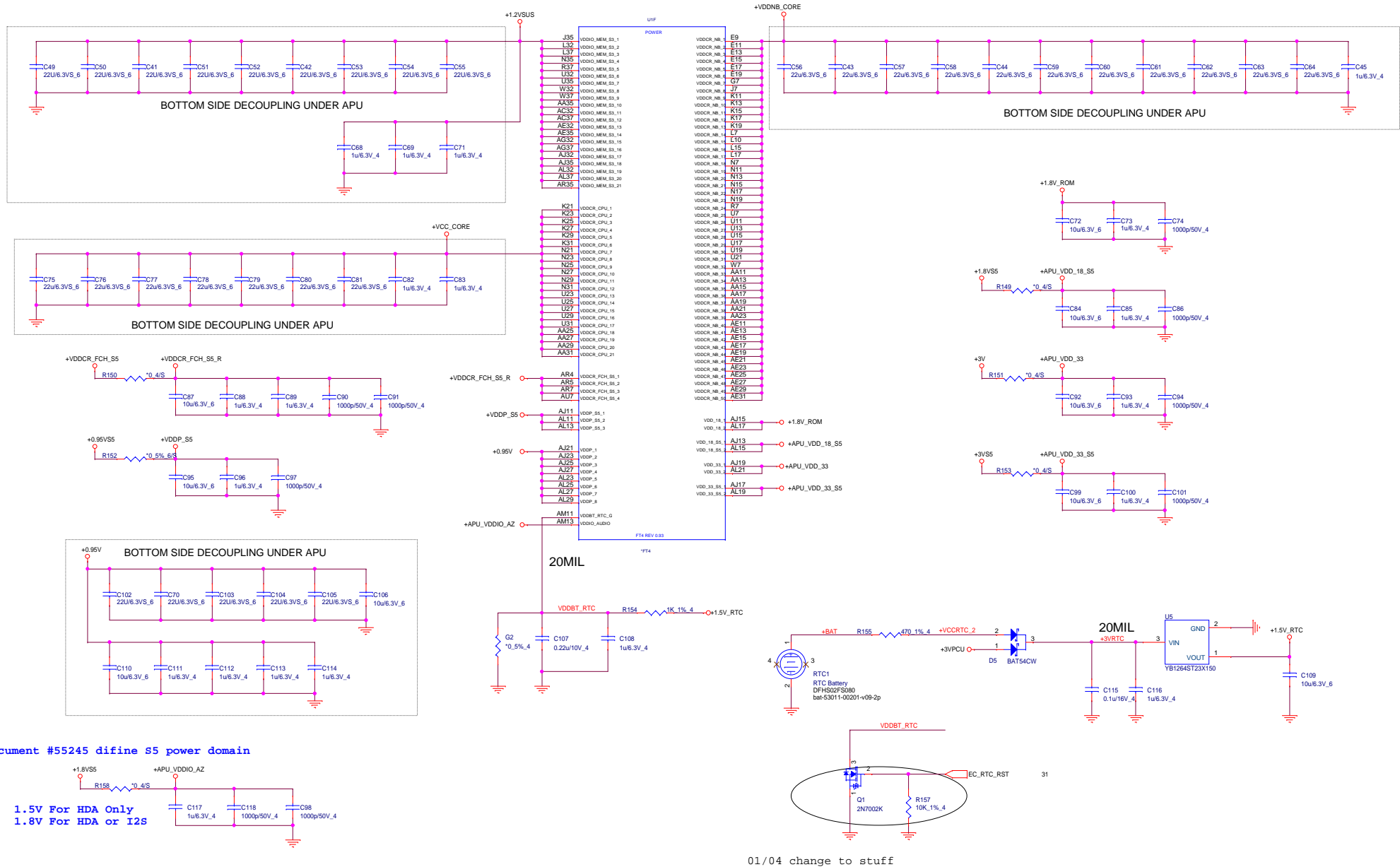
## Follow Checklist

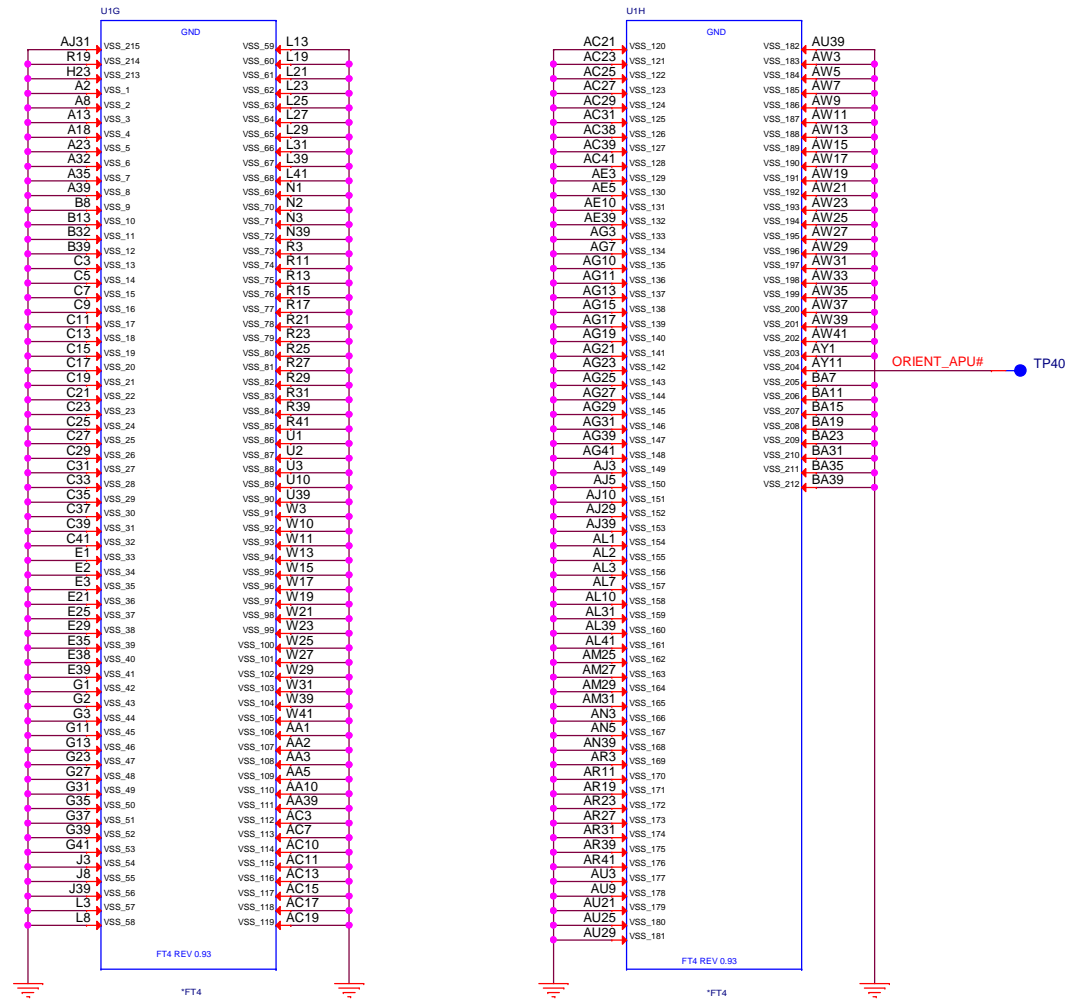


## Follow Checklist



**Power Decoupling follow Check list by AMD suggestion**






**PROJECT : Rams 0P2/0P2A**  
**Quanta Computer Inc.**

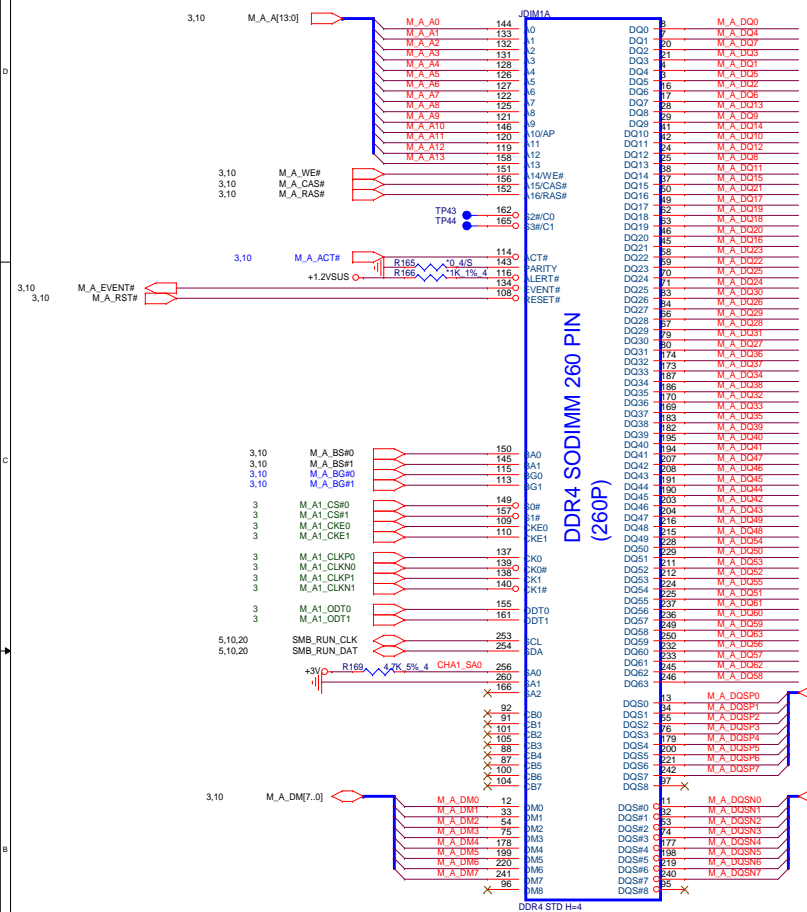
Size	Document Number	Rev
	<b>ST 717 (GND)</b>	1A
Date: Wednesday, March 08, 2017	Sheet	8 of 48



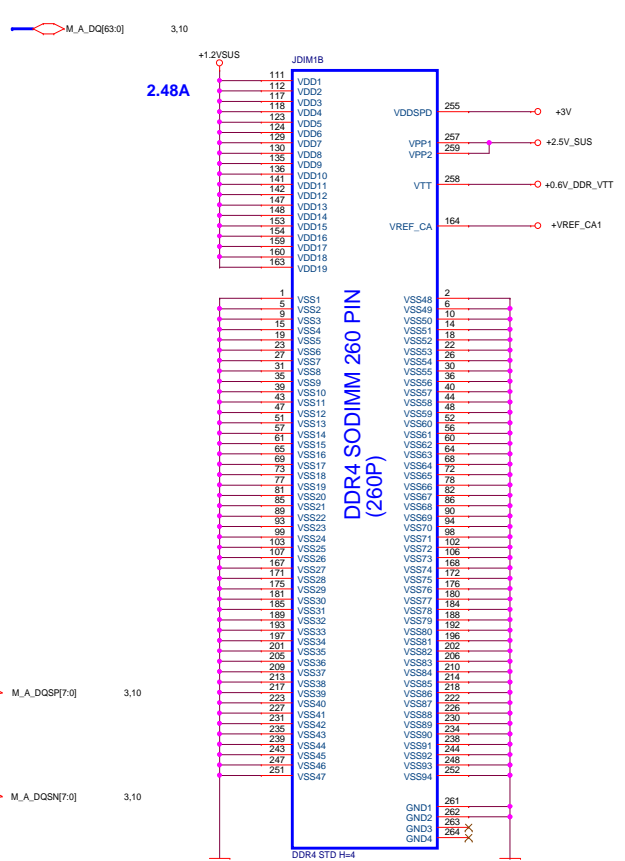
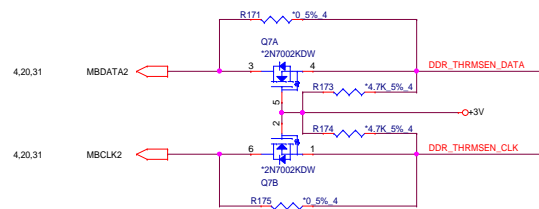
<Reserved>

 <b>NB5</b>	<b>PROJECT : Rams 0P2/0P2A</b> Quanta Computer Inc.		
	Size A	Document Number <b>Reserved</b>	Rev 1A
	Date: Wednesday, March 08, 2017    Sheet 9 of 48		

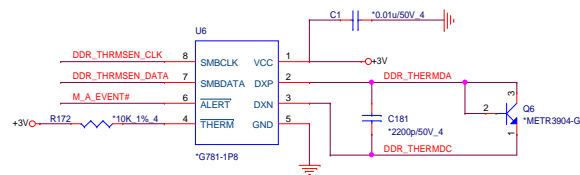




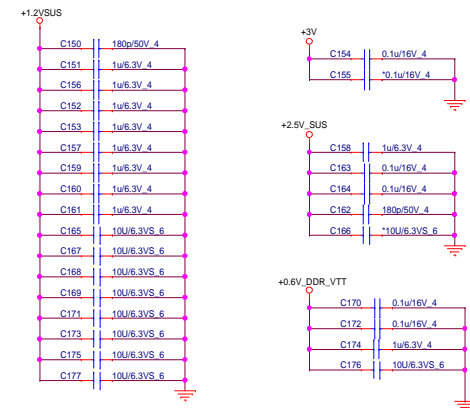
### **Local Thermal Sensor**



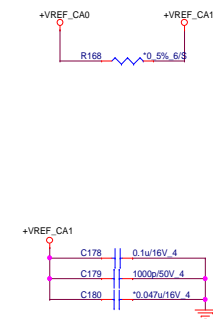
Main:AL000781039	G781-1P8(9Ah)
2nd:AL001412005	EMC1412-2-ACZL-TR(9Ah)
Main:AL001412003	EMC1412-1-ACZL-TR(98h)
2nd:AL000431014	TMP431ADGKR(98h)



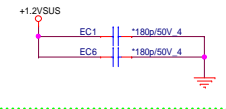
**Place these Caps near SODIMM**




1uF/10uF 4pcs on each side of SODIMM

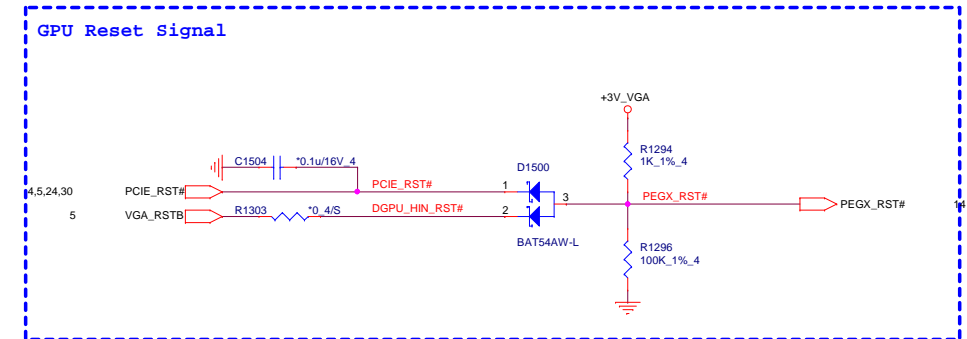
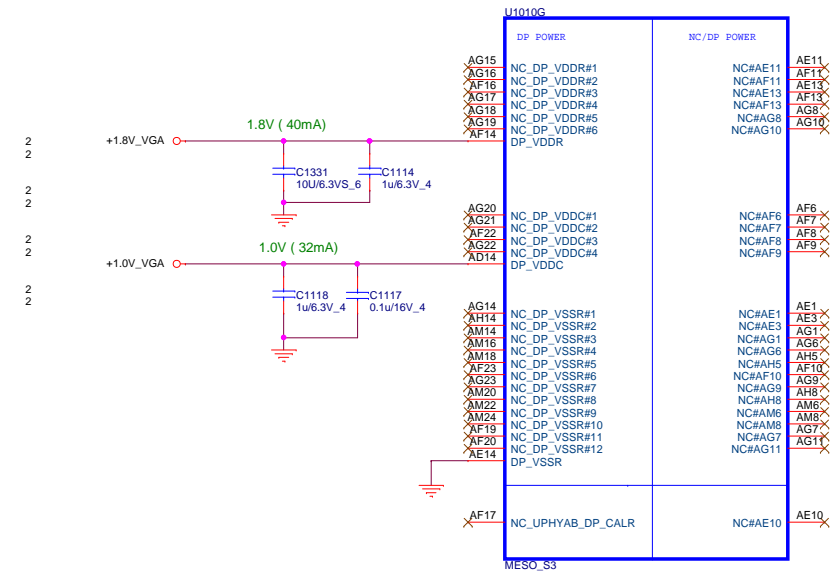
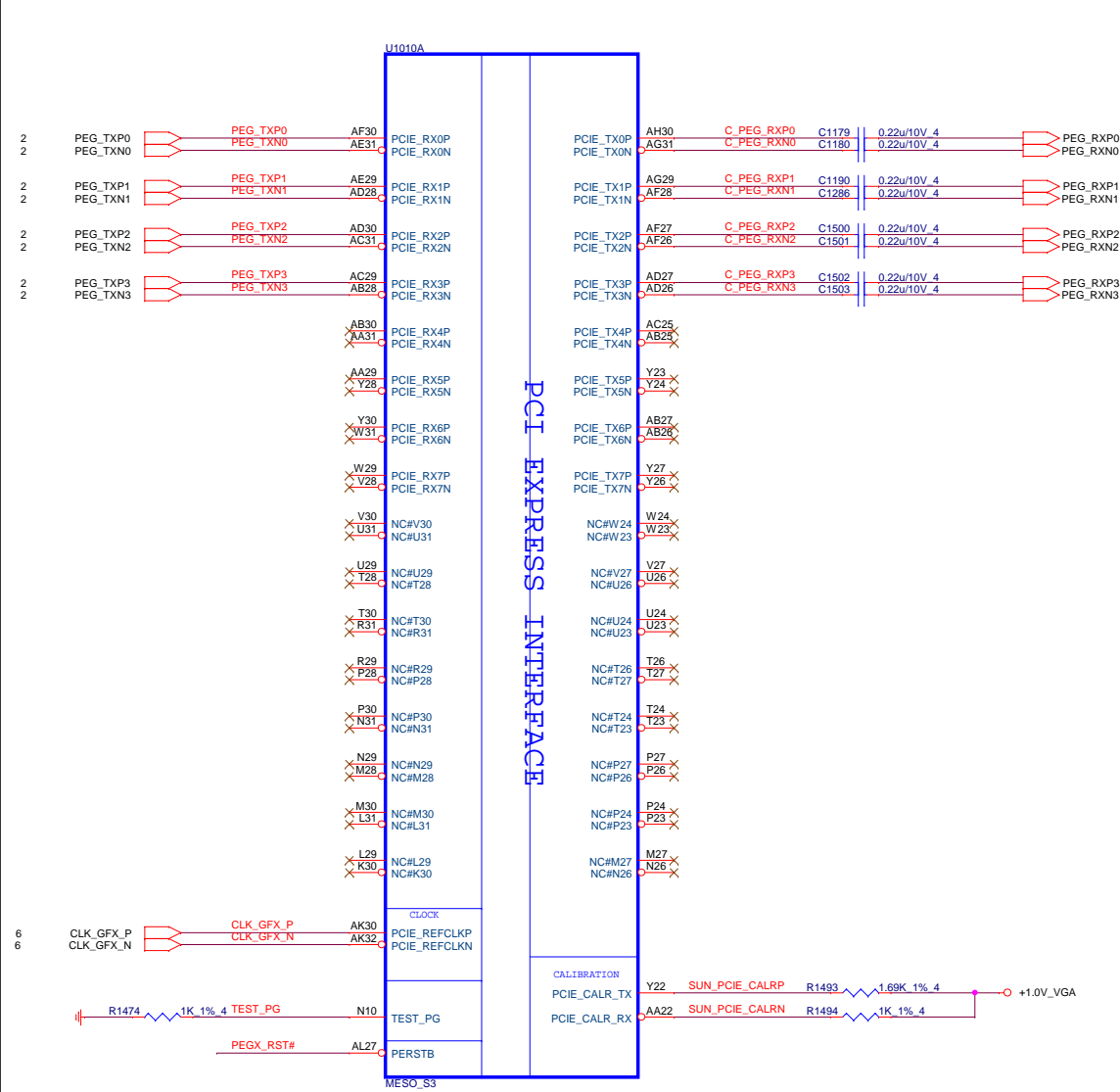


For EMI CAP



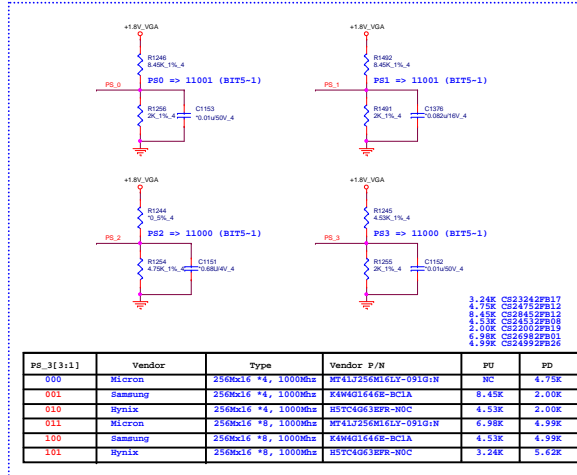
<Reserved>

 NB5	<b>PROJECT : Rams 0P2/0P2A</b> Quanta Computer Inc.		
	Size A	Document Number <b>Reserved</b>	Rev 1A
	Date: Wednesday, March 08, 2017    Sheet 12 of 48		



**PROJECT : Rams OP2/OP2A**  
Quanta Computer Inc.

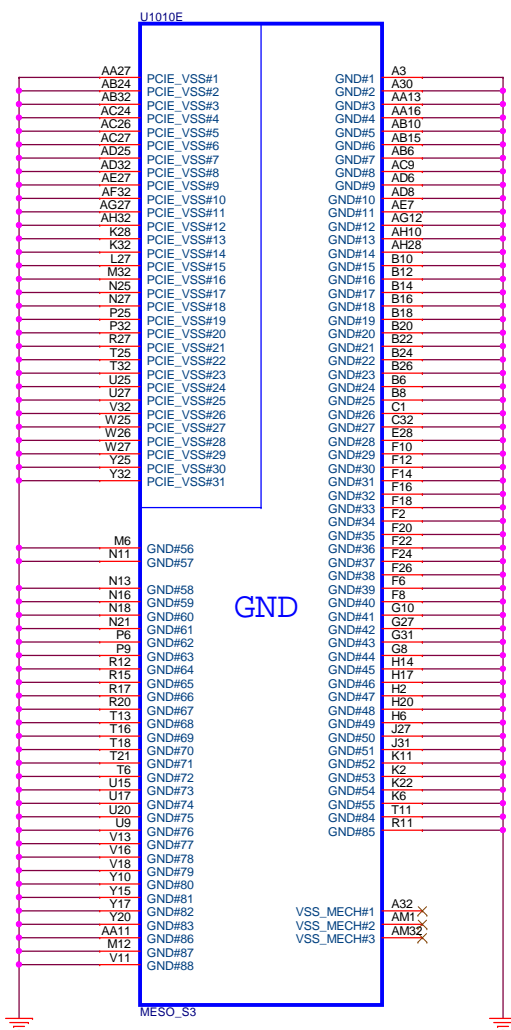
Size	Document Number	Rev
	<b>M1-70_S3_PCIE/DP POWER</b>	1A
Date: Wednesday, March 08, 2017	Sheet	13 of 48



Size of the Primary Memory Apertures	ROM CONFIG[2:0]
--------------------------------------	-----------------

128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

MLP Bit	Strap Name	Description	Recommended Settings
PS_001	ROM_CONFIG01	If STRAP_ROM_EN = 1 ROM_CONFIG01 can influence the ROM type.	Design dependent, see the description
PS_002	ROM_CONFIG01	If STRAP_ROM_EN = 0 ROM_CONFIG01 defines the primary memory aperture size. See February Security Notes page 5.	
PS_046	N/A	Reserved for internal use only. Never bit at 1 set.	1
PS_081	N/A	Reserved.	1
PS_082	STRAP_GEN_GENEN_A	PC1 GENEN capability. 0 = PC1 GENEN is supported. 1 = PC1 GENEN is not supported. Determines whether or not the PC1-references clock frequency is reported in the P1 configuration space under the GENEN bit in CLDR01.	Design dependent, see the description
PS_124	STRAP_GEN_CLKEN_EN	0 = The CLDR01 power management capability is disabled. 1 = The CLDR01 power management capability is enabled.	0
PS_133	N/A	Reserved for internal use only. Never bit at 0 set.	0
PS_144	STRAP_TX_CDO_RAP_PULL_EN	Control the transmitter full-RAP swing mode. 0 = The transmitter full swing is enabled. 1 = The transmitter full swing is disabled.	0
PS_151	STRAP_TX_BRENNEN_EN	PC1 EXPRES (transmitter, describable) enabled. 0 = Tx descregnal disabled. 1 = Tx descregnal enabled.	Design dependent, see the description
PS_201	N/A	Reserved.	0
PS_202	N/A	Reserved.	0
PS_204	STRAP_ROM_ROM_EN	To enable the external ROM. 0 = Disable the external ROM. 1 = Enable the external ROM. 0 = Enable the external ROM. 1 = Enable the external ROM. ROM device.	Design dependent, see the description
PS_246	N/A	Reserved.	1
PS_248	N/A	Reserved.	1
PS_312	BOARD_CONFIG01	Board configuration related variables such as memory type.	Design dependent, see the description
PS_313	BOARD_CONFIG01	Board configuration related variables such as memory type.	
PS_351	N/A	Reserved.	0
PS_352	N/A	Reserved.	0



# CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS  
0= DO NOT INSTALL RESISTOR  
1 = INSTALL 3K RESISTOR  
X = DESIGN DEPENDANT  
NA = NOT APPLICABLE

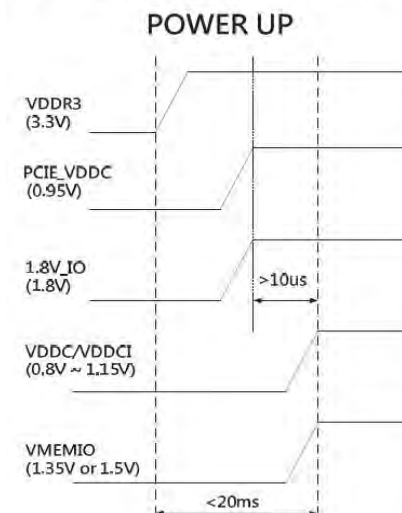
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

## NOTE1: AMD RESERVED CONFIGURATION STRAPS

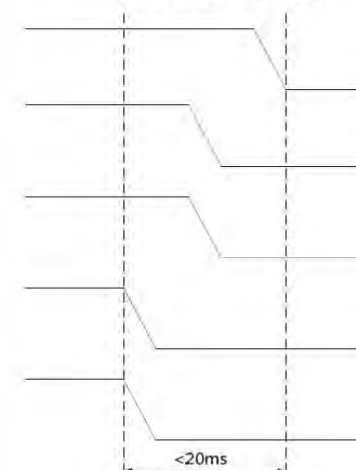
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

## POWER UP / POWER DOWN SEQUENCE

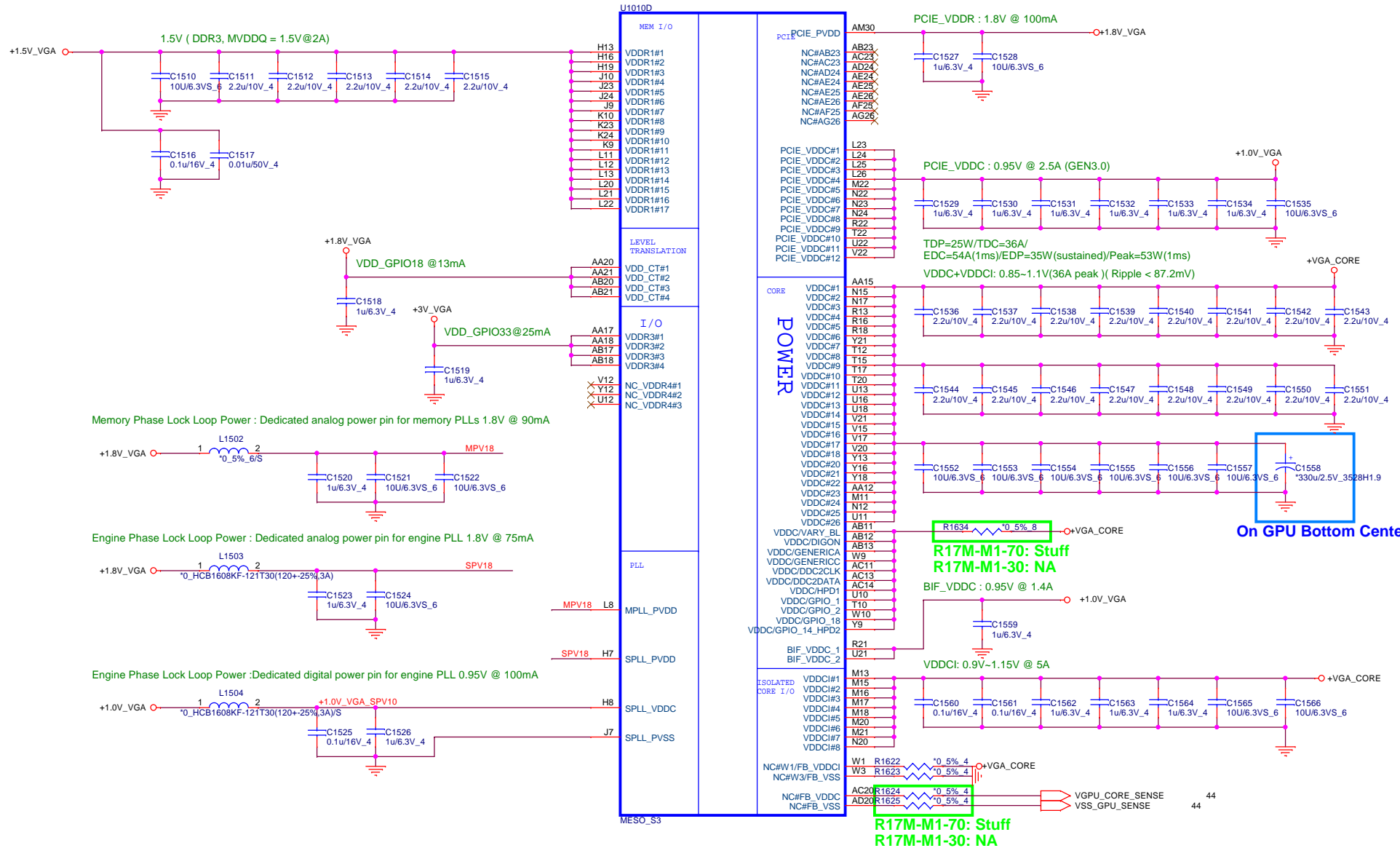


## POWER DOWN



**PROJECT : Rams OP2/OP2A**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>M1-70_S3_GND/LVDS/Strap</b>	1A
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**PROJECT : Rams 0P2/0P2A**  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>M1-70_S3_POWER</b>	1A
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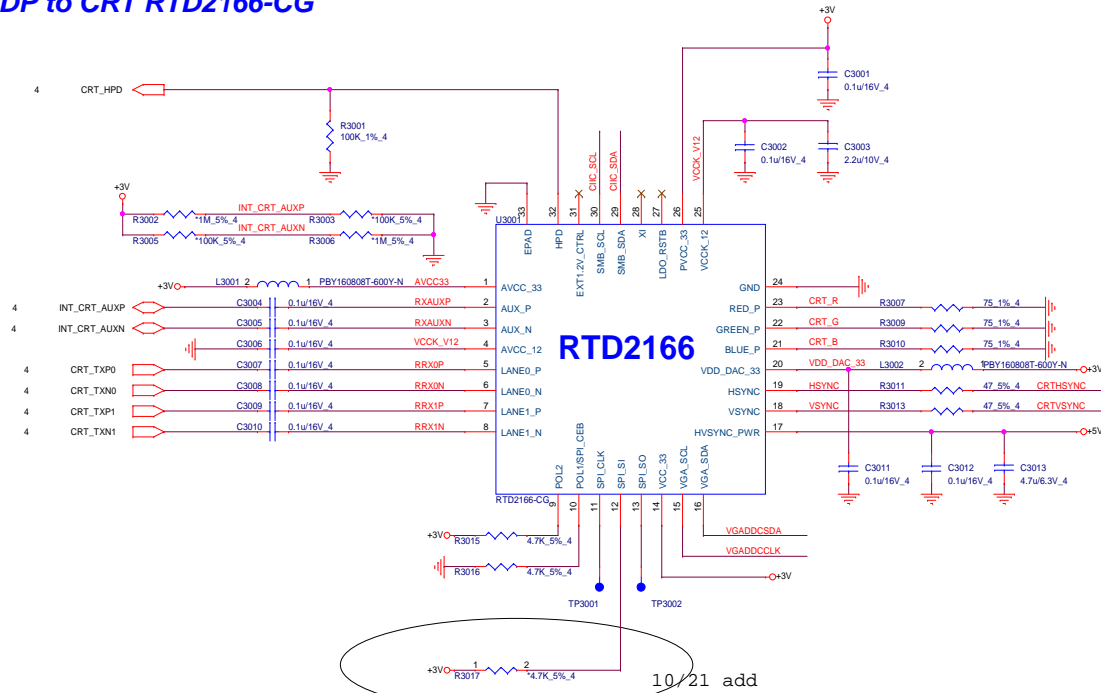








## DP to CRT RTD2166-CG



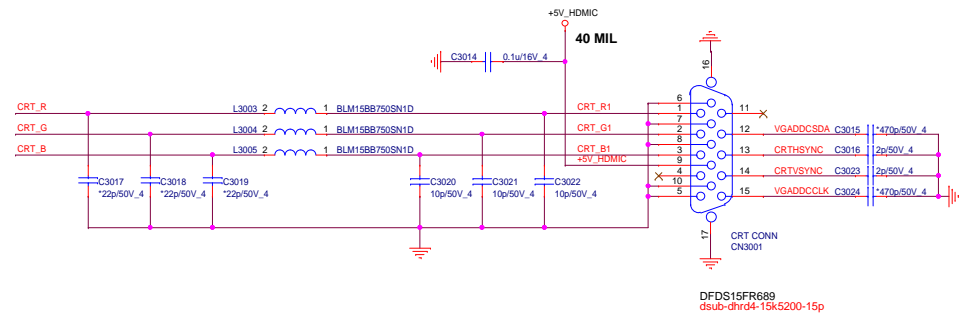
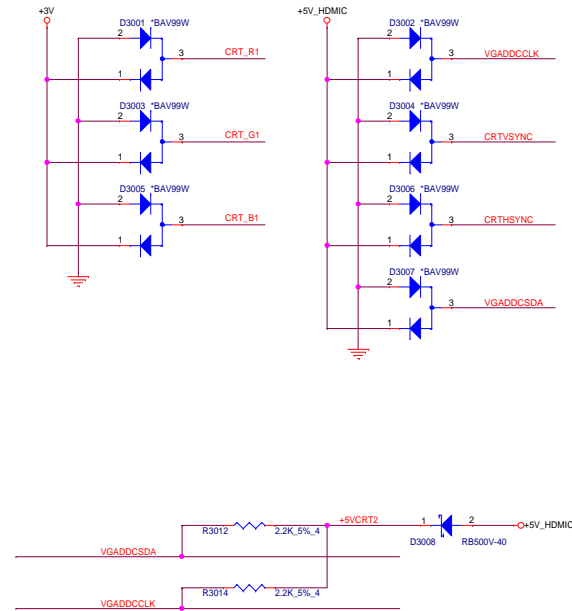
## CIIC\_SCL, CIIC\_SDA Connection

EP mode: Pin2, Pin3 connect to EC SMBUS  
 ROM or EEPROM mode: connect to PCH SMBUS  
 IIC Protocol is used

## From PCH



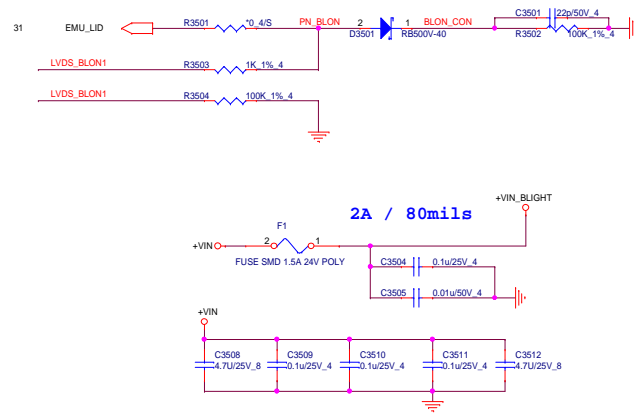
## From EC



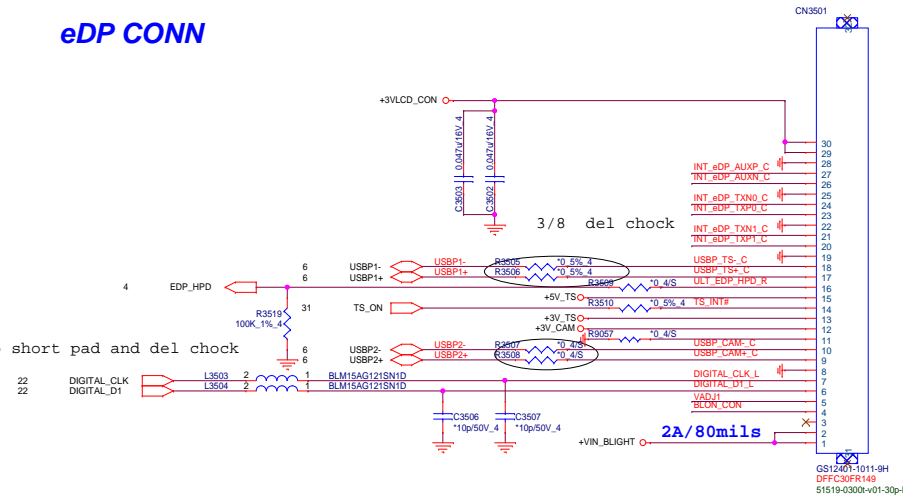
**PROJECT : Rams 0P2/0P2A**  
**Quanta Computer Inc.**

Size C Document Number DP to CRT RTD2166-CG Rev 1A  
 Date: Wednesday, March 08, 2017 Sheet 20 of 48

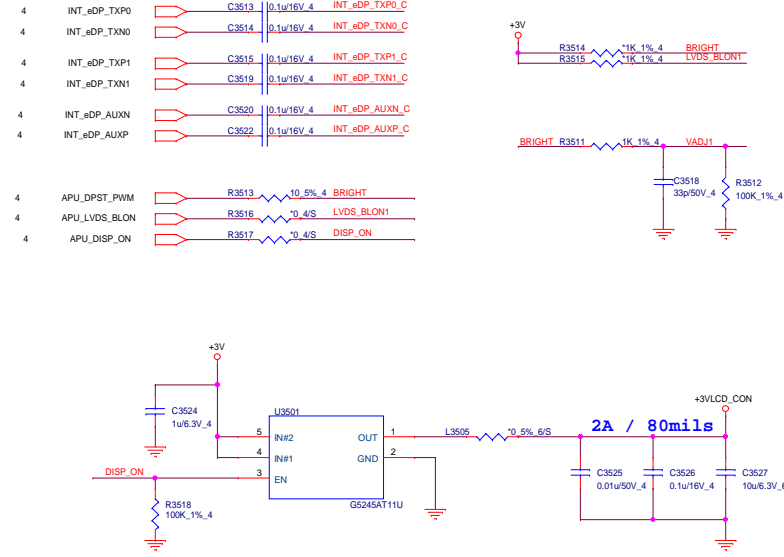
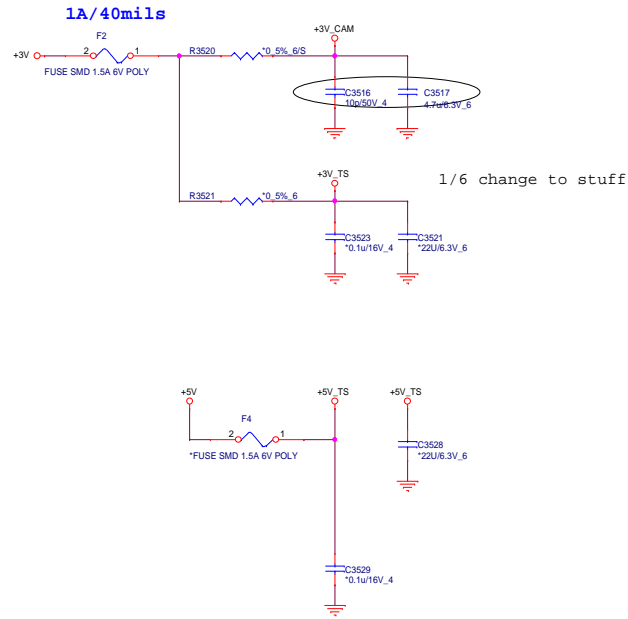
## LID Switch

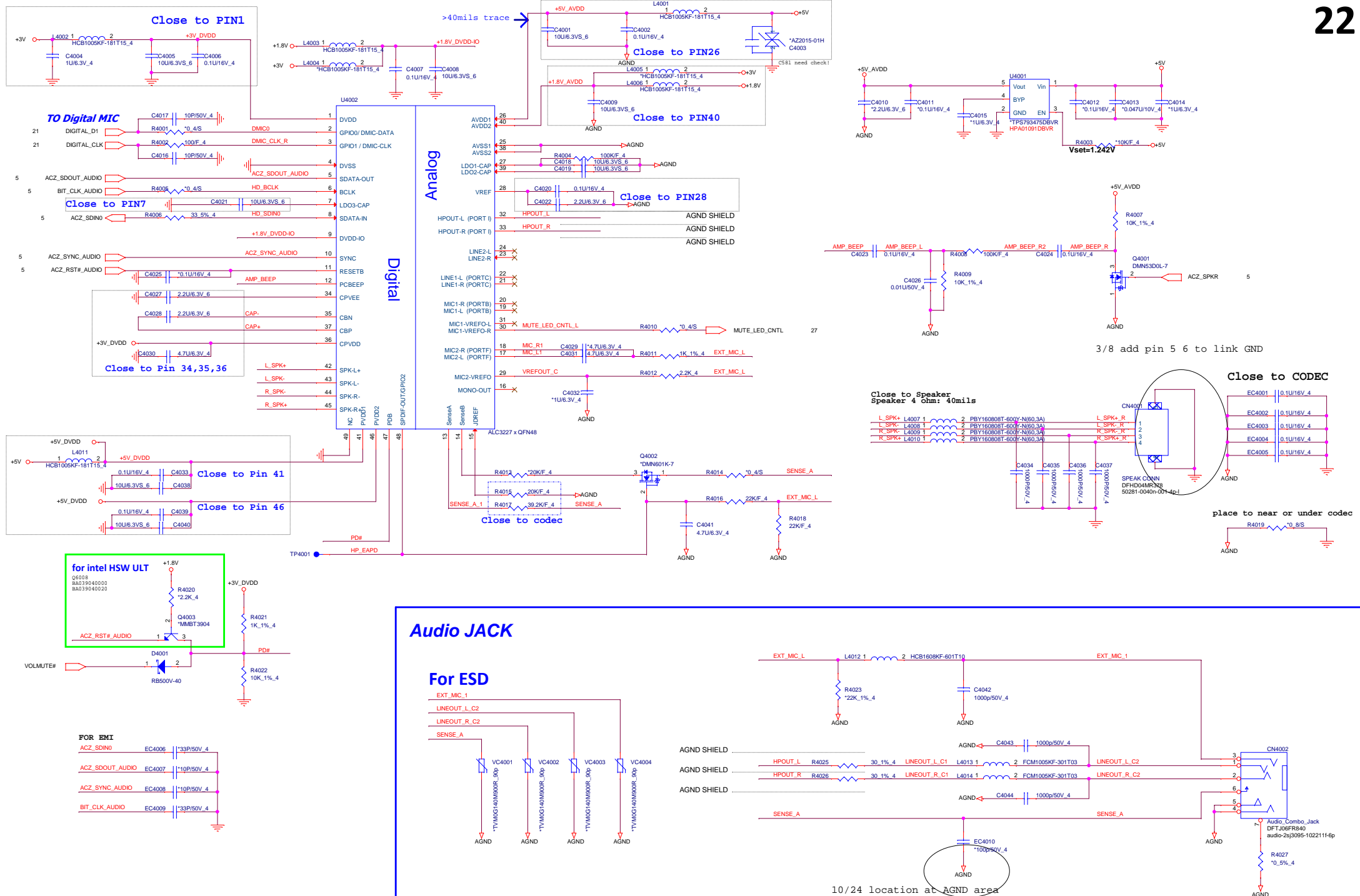


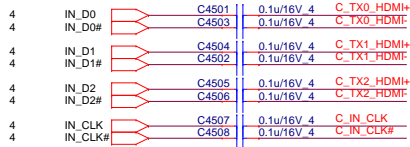
**eDP CONN**



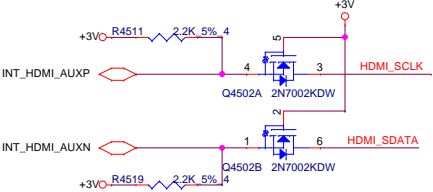
## Touch screen



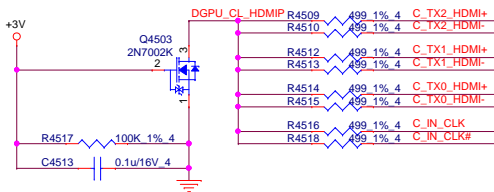




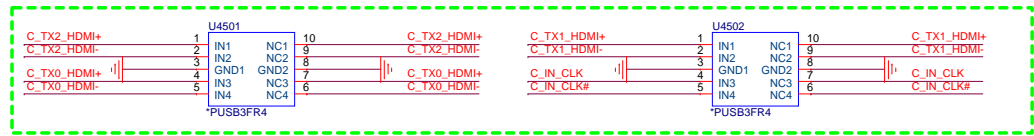
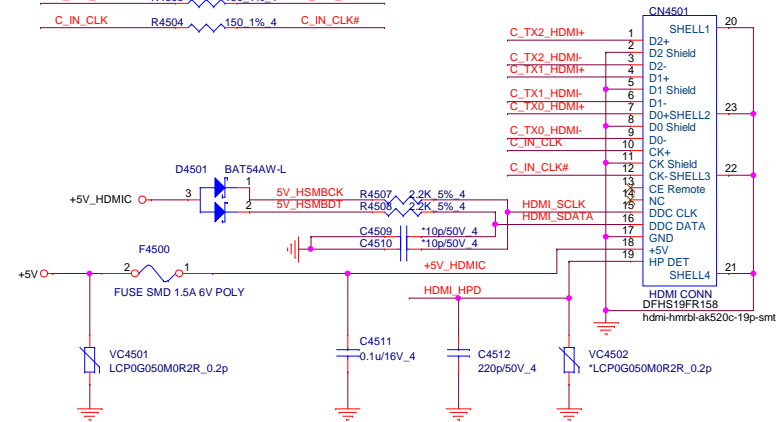
HDMI SMBus Isolation



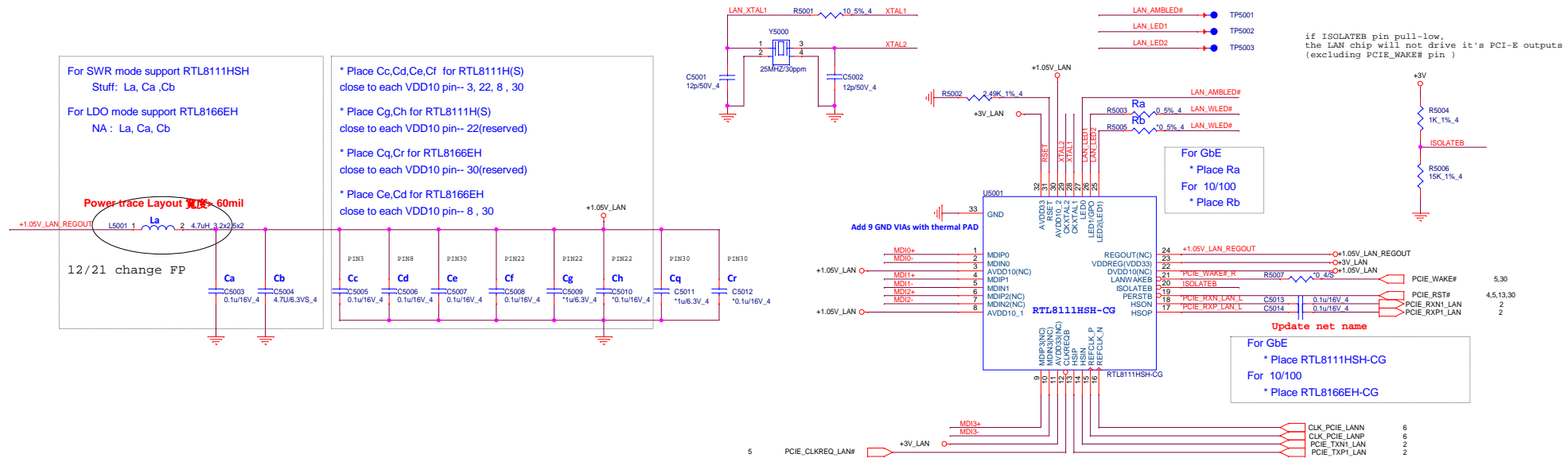
Close to HDMI connector



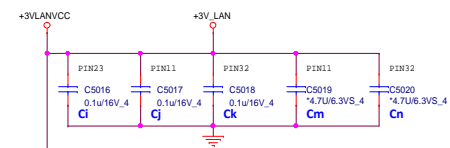
EMI Solution



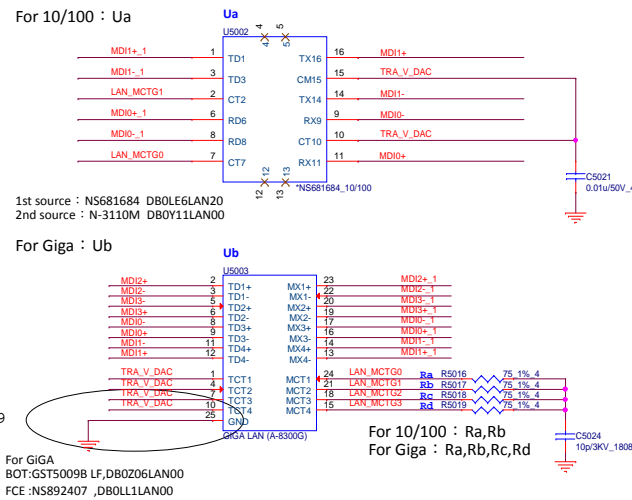




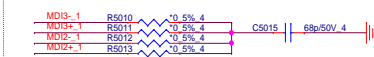
- \* Place Ci and Ck, close to each VDD33 pin-- 23, 32 for RTL8166EH
- \* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for RTL8111H(S)
- \* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)



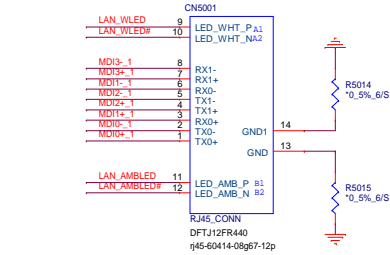
12/21 del R9058 R9059



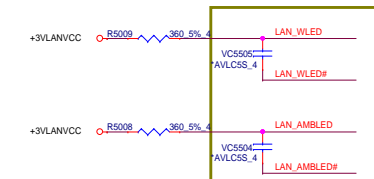
For 10/100 stuff only & Close RJ45



RJ45: DFTJ12FR440 LED amber (Pin9/10) & white (Pin11/12)



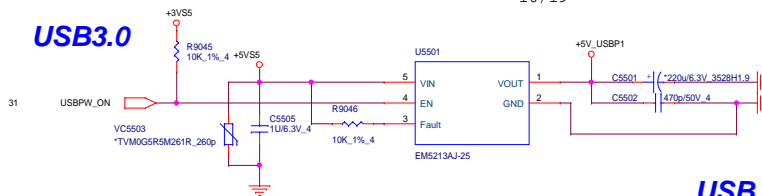
SI



For 10/100 : ESD1  
For Giga : ESD1,ESD2

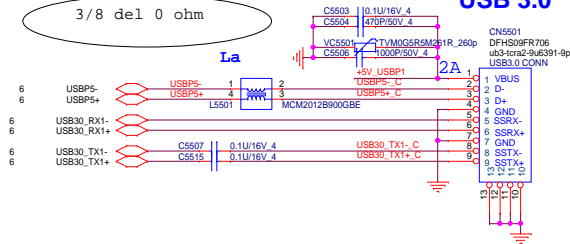
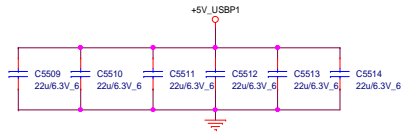


## USB3.0



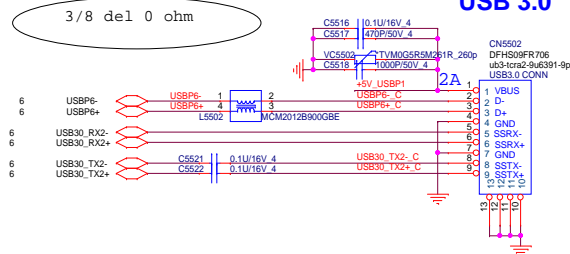
## USB 2.0/3.0 Combo

## USB 3.0

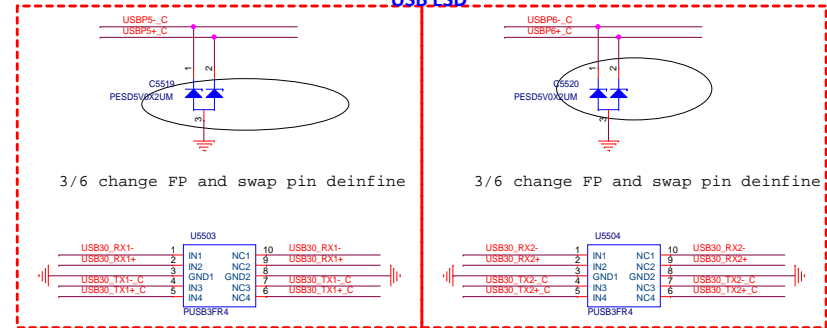


## USB 2.0/3.0 Combo

## USB 3.0

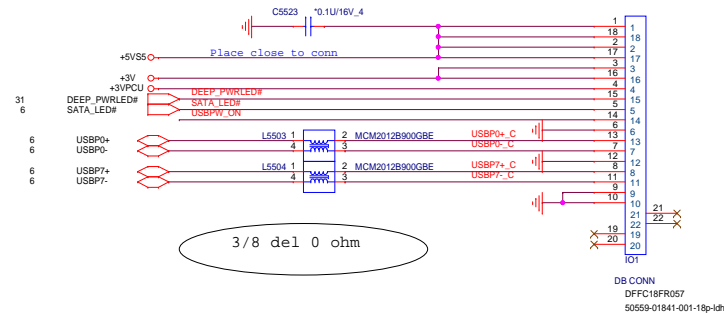


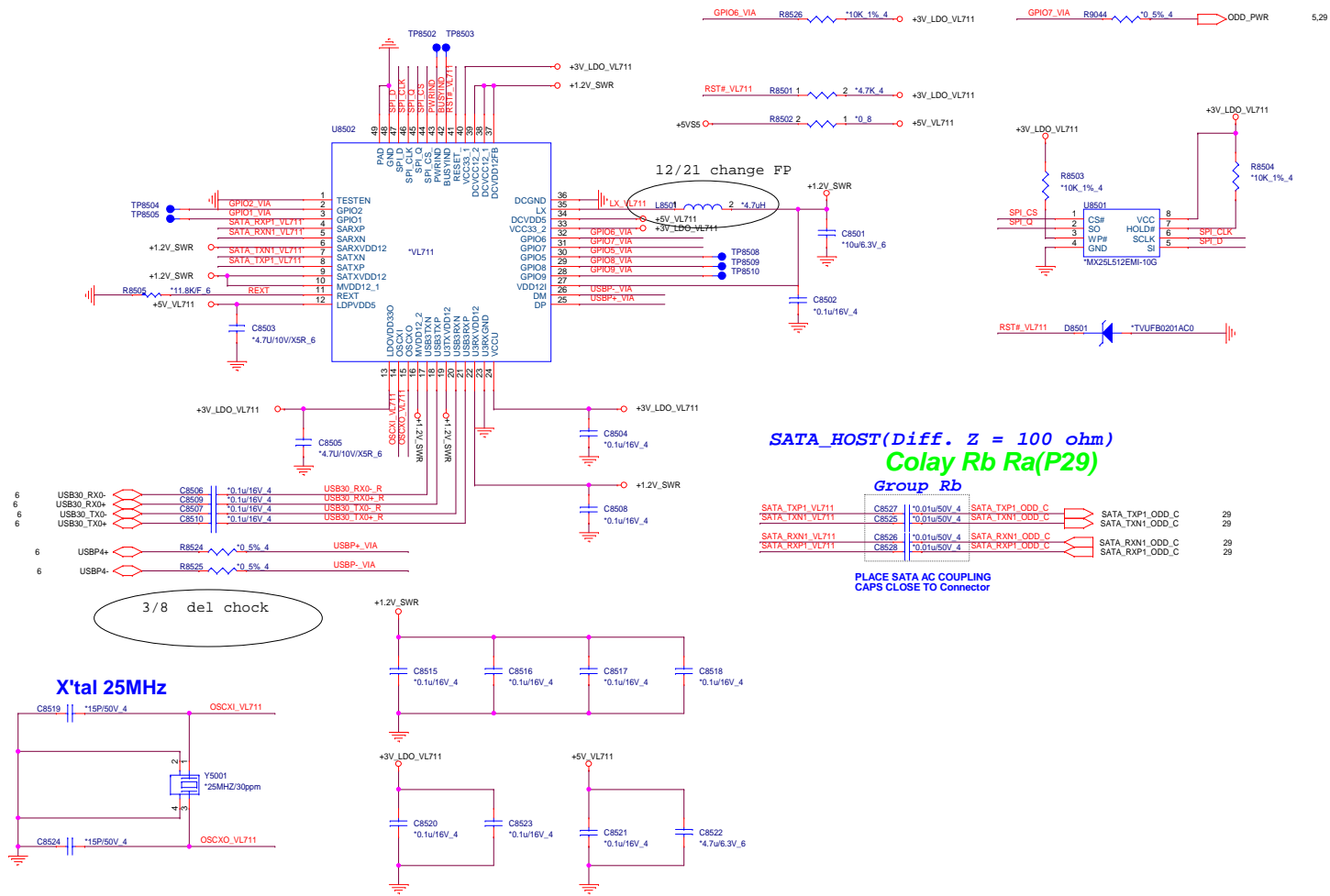
## USB ESD



## Daughter Board

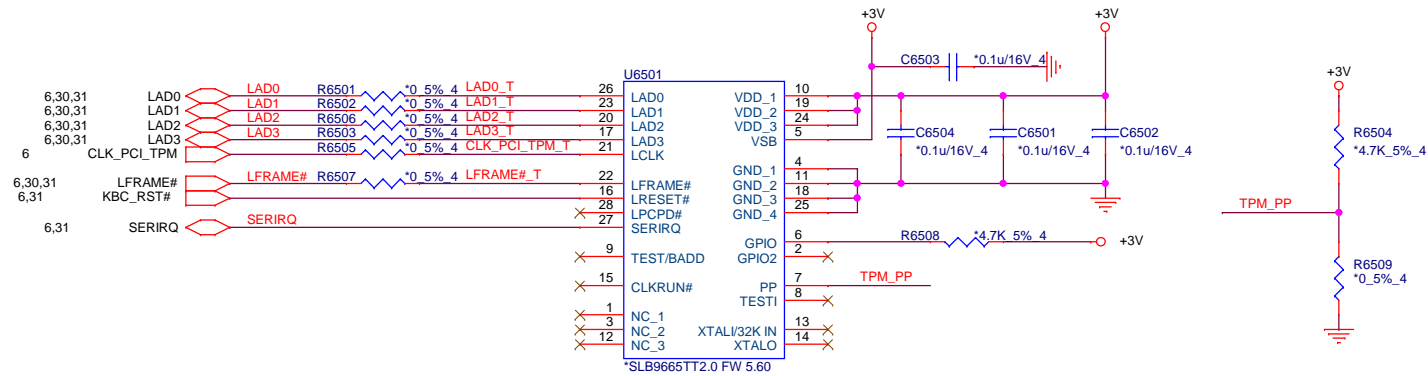
USB2.0 CONN ON DB  
Card Reader





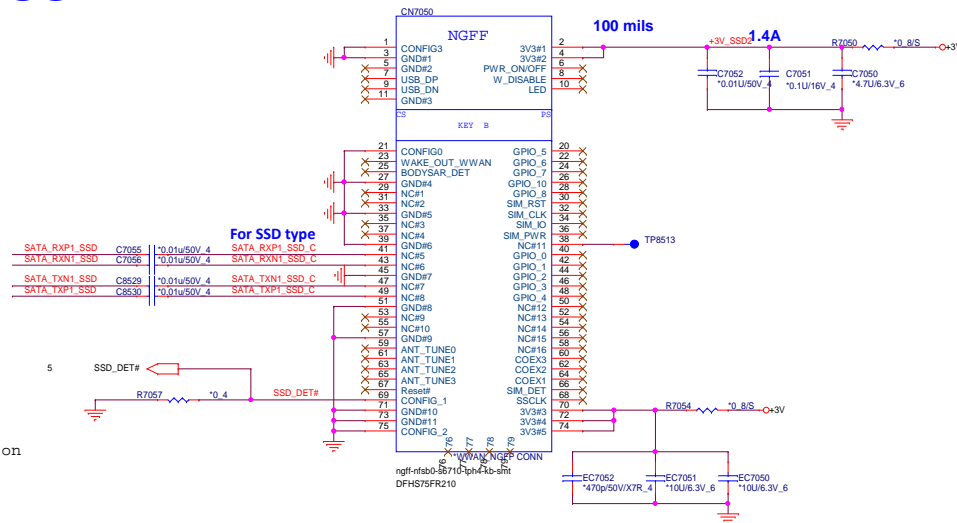


# TPM



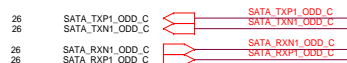
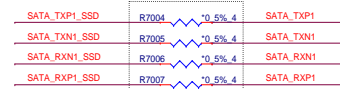
**PROJECT : Rams 0P2/0P2A**  
Quanta Computer Inc.

Size B	Document Number <b>TPM</b>	Rev 1A
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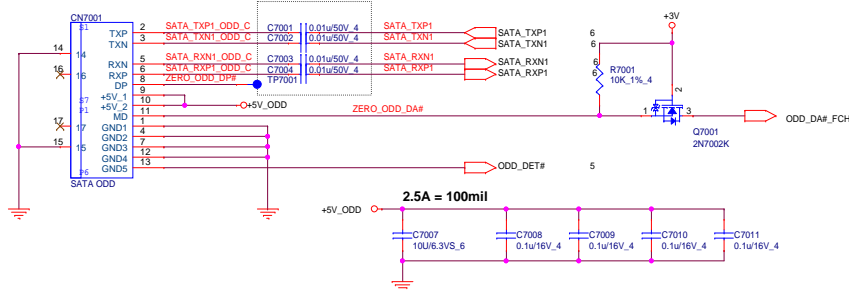
## Group Rb

Close ODD side, Colay Top / Bot side for branch!!



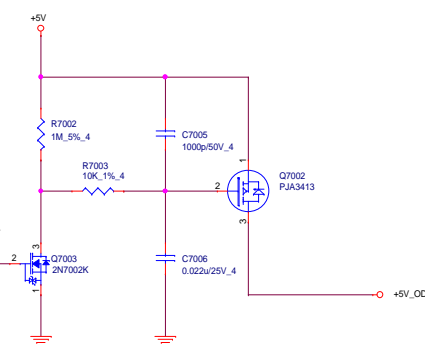
## SATA ODD Colay Ra Rb(P26)

### Group Ra

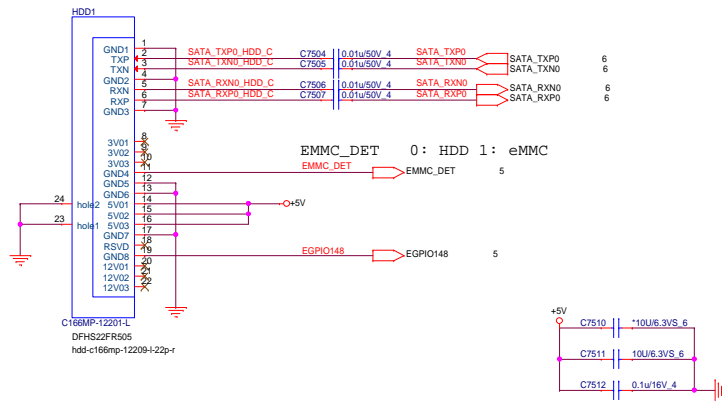


High : ODD power on  
Low : ODD power down

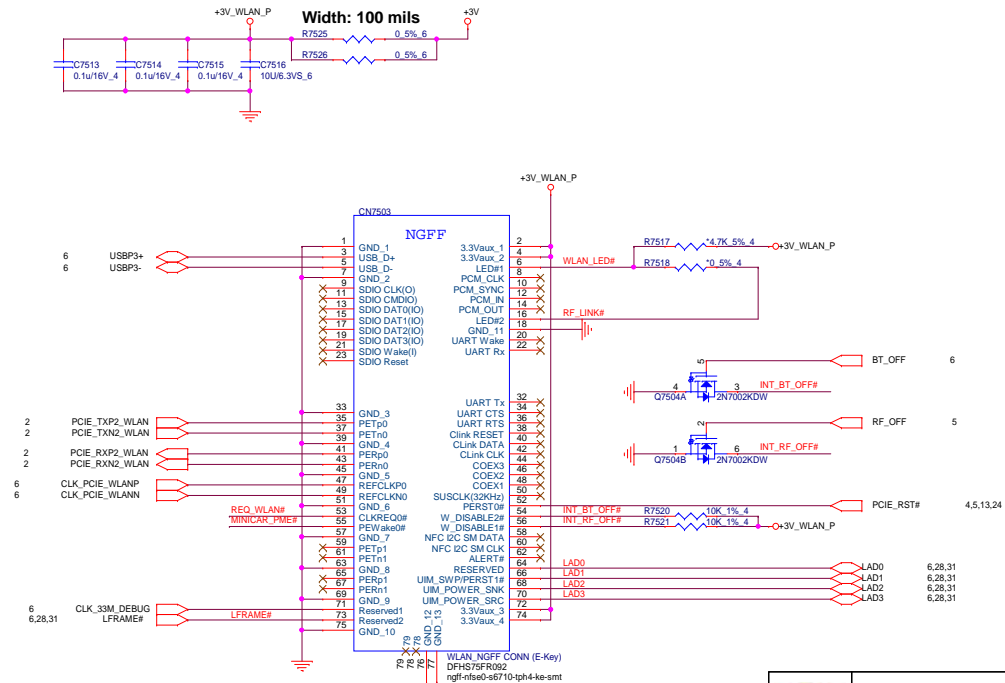
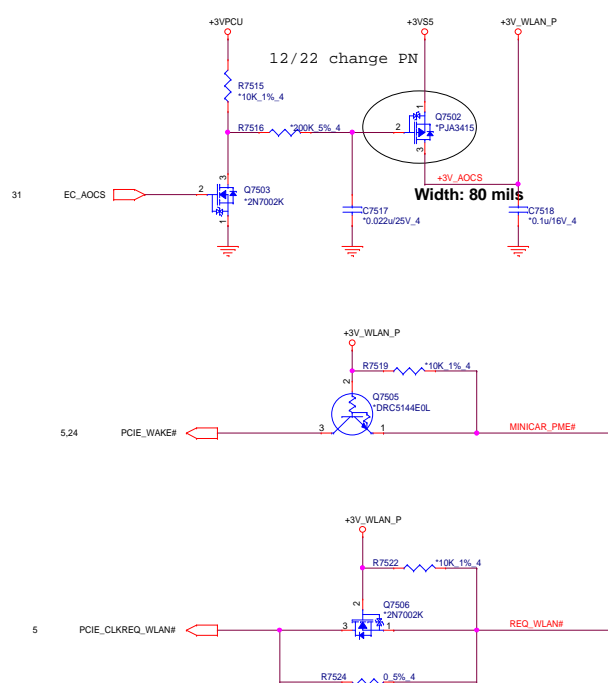
5.26 ODD\_PWR

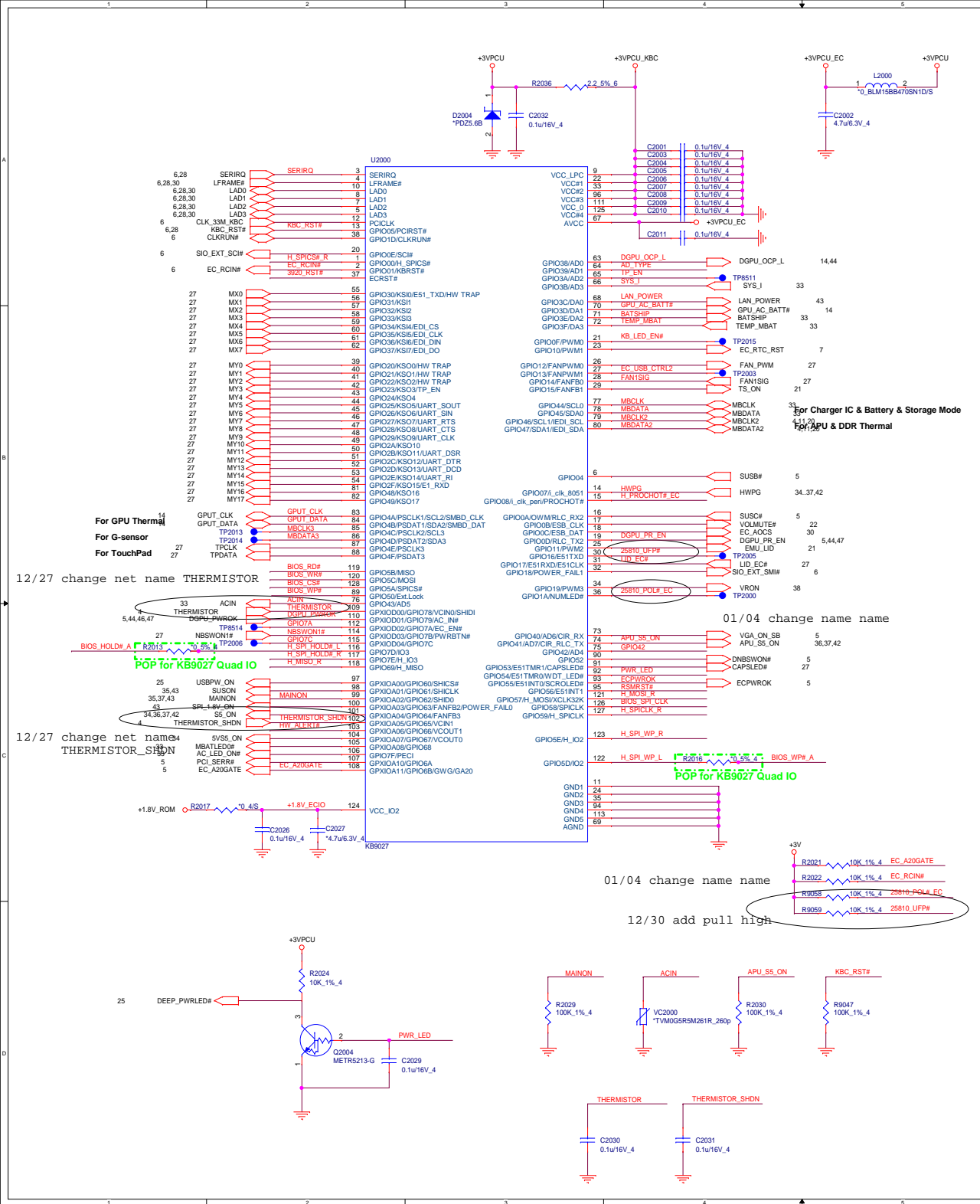


## SATA HDD



## WLAN & BT

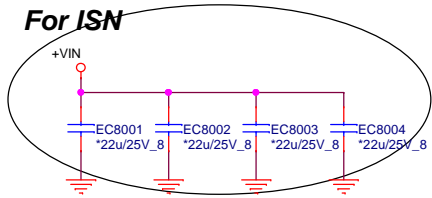




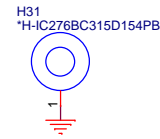
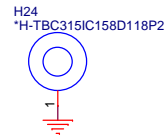
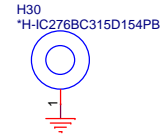
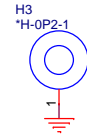
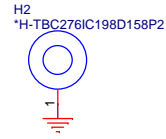
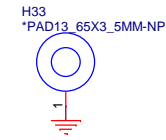
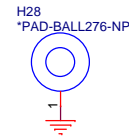
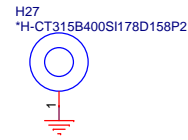
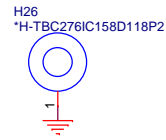
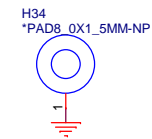
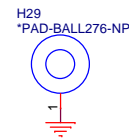
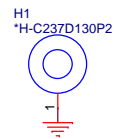
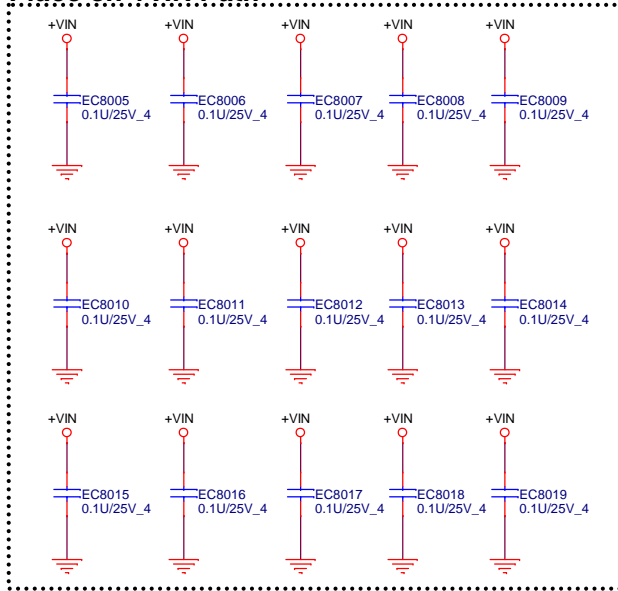
# EMI CAPs

10/20 change +PRWSRC to +VIN

## For ISN



## Place on +VIN Path



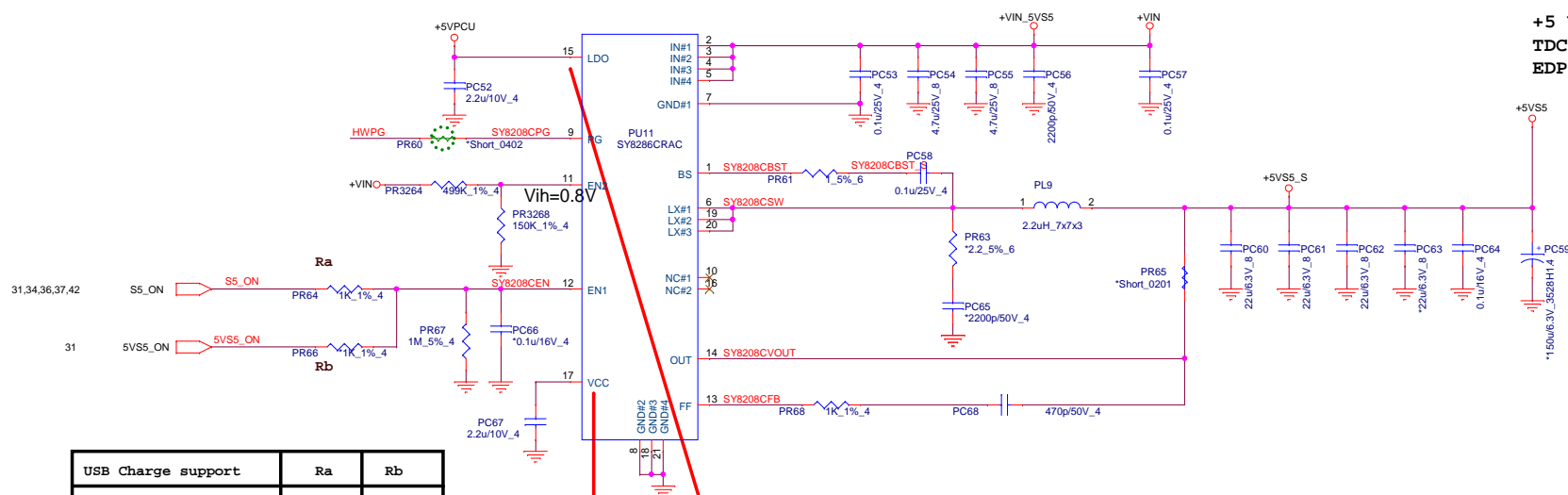
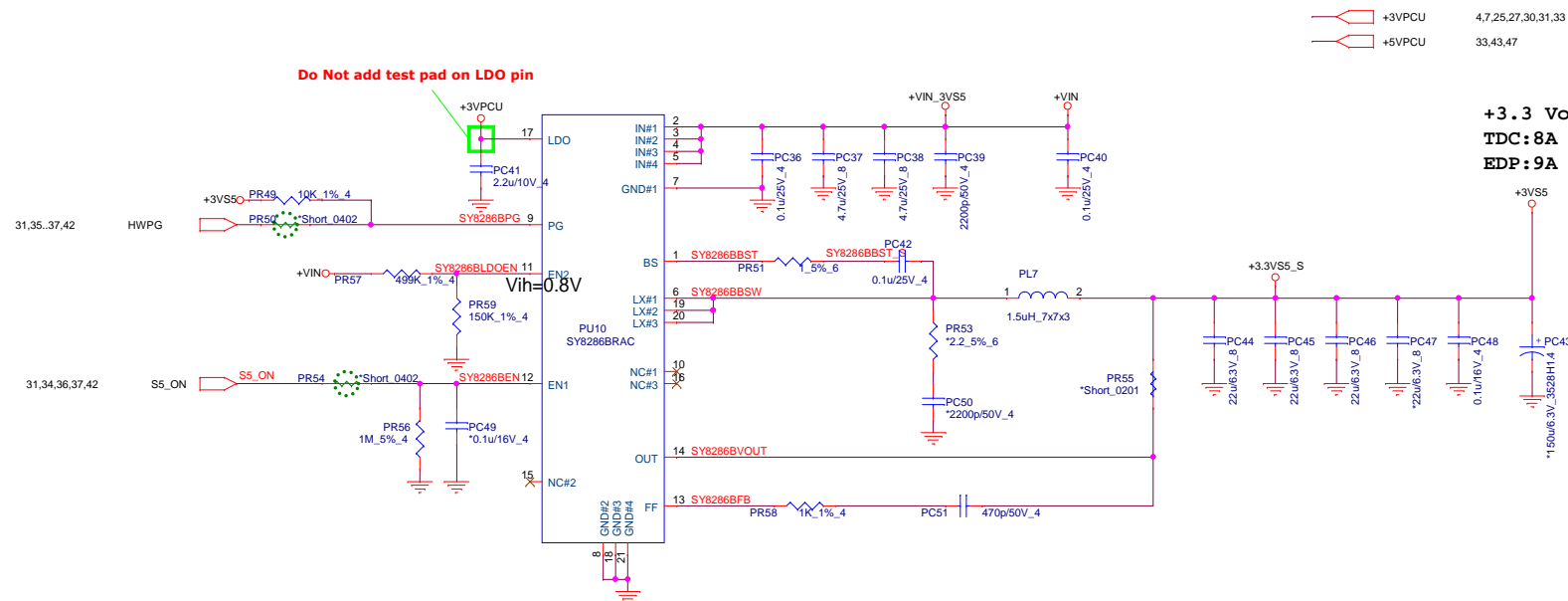
32



<b>PROJECT : Rams OP2/OP2A</b> Quanta Computer Inc.		
Size B	Document Number <b>EMI CAP/HOLES</b>	Rev 1A
Date: Wednesday, March 08, 2017	Sheet	32 of 48



Size Custom	Document Number <b>Charger (BQ24728H)</b>	Rev 1A
Date: Wednesday, March 08, 2017		Sheet 33 of 46

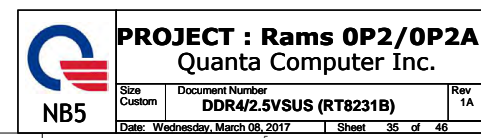


USB Charge support	Ra	Rb
Pavilion (No support)	Stuff	NA
Envy (Support)	NA	Stuff

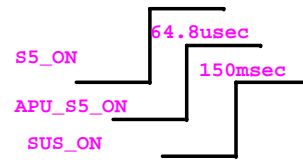
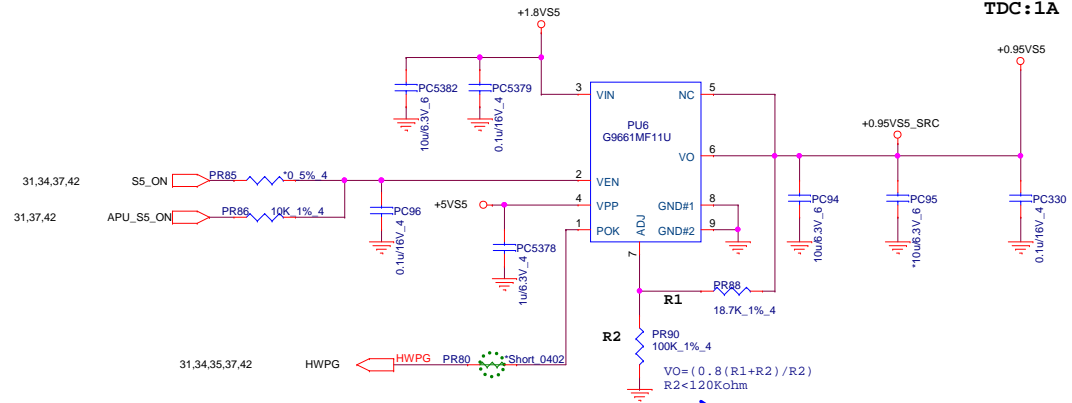
**Do Not add test pad on VCC & LDO pin**

**PROJECT : Rams OP2/OP2A**  
**Quanta Computer Inc.**

Size Custom	Document Number 3/VS5 (SY8286B/SY8286C)	Rev 1A
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+0.95V +/- 5%  
TDC:1A

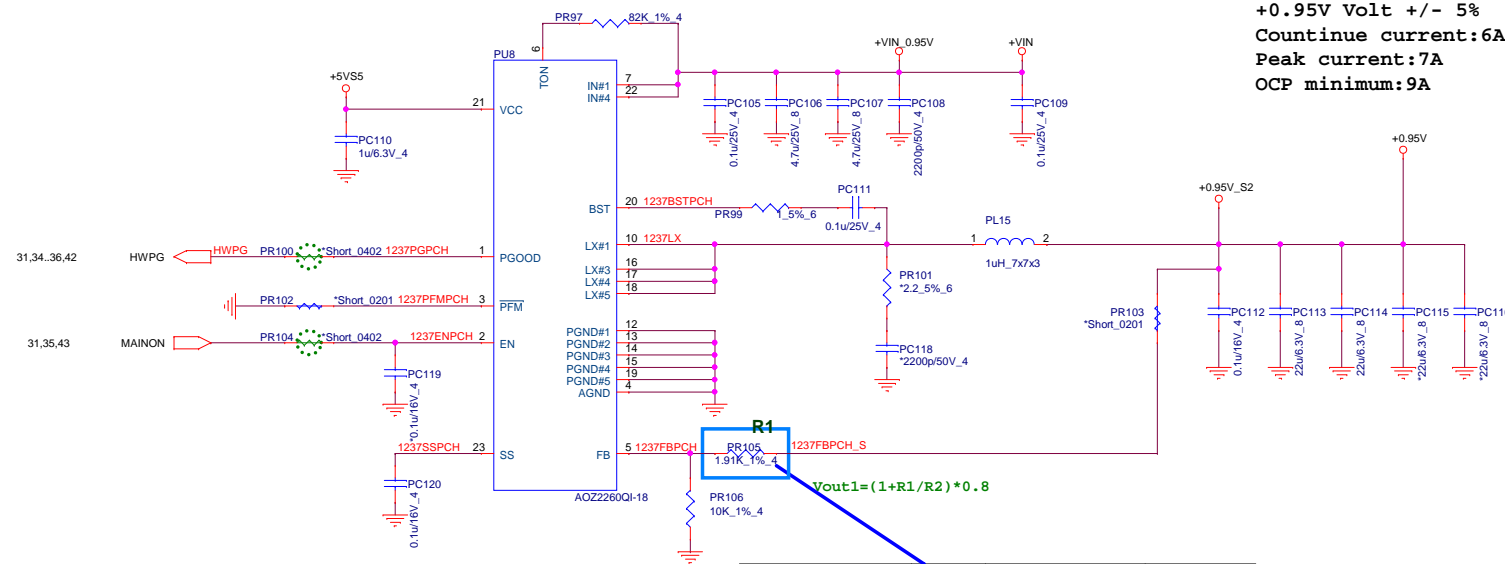


R1			
	R1		
Stoney/Bristol	18.7K	CS31872FB19	0.95V
	31.6K	CS33162FB14	1.05V

Bristol VDDP=1.05V  
Stoney VDDP=0.95V

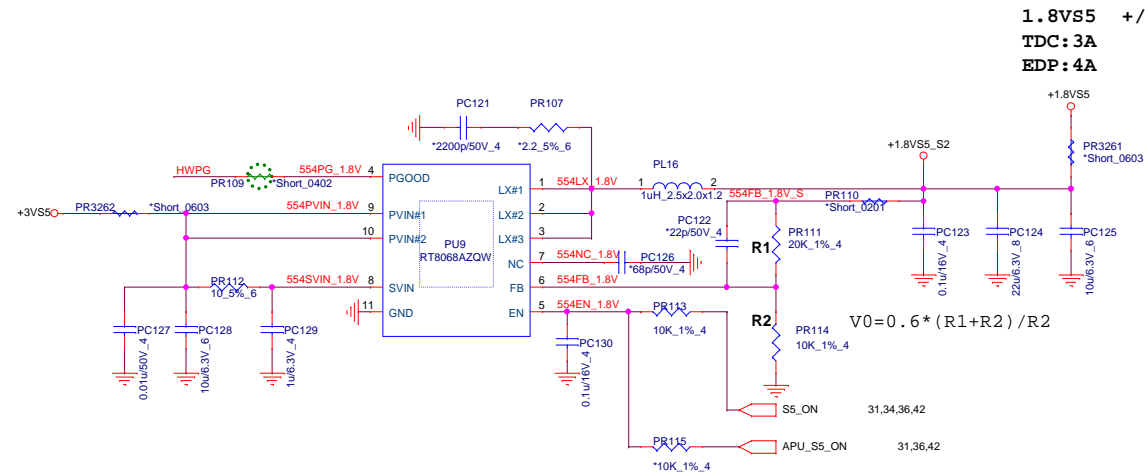
**PROJECT : Rams OP2/OP2A**  
Quanta Computer Inc.

Size Custom	Document Number <b>+0.95VS5</b>	Rev 1A
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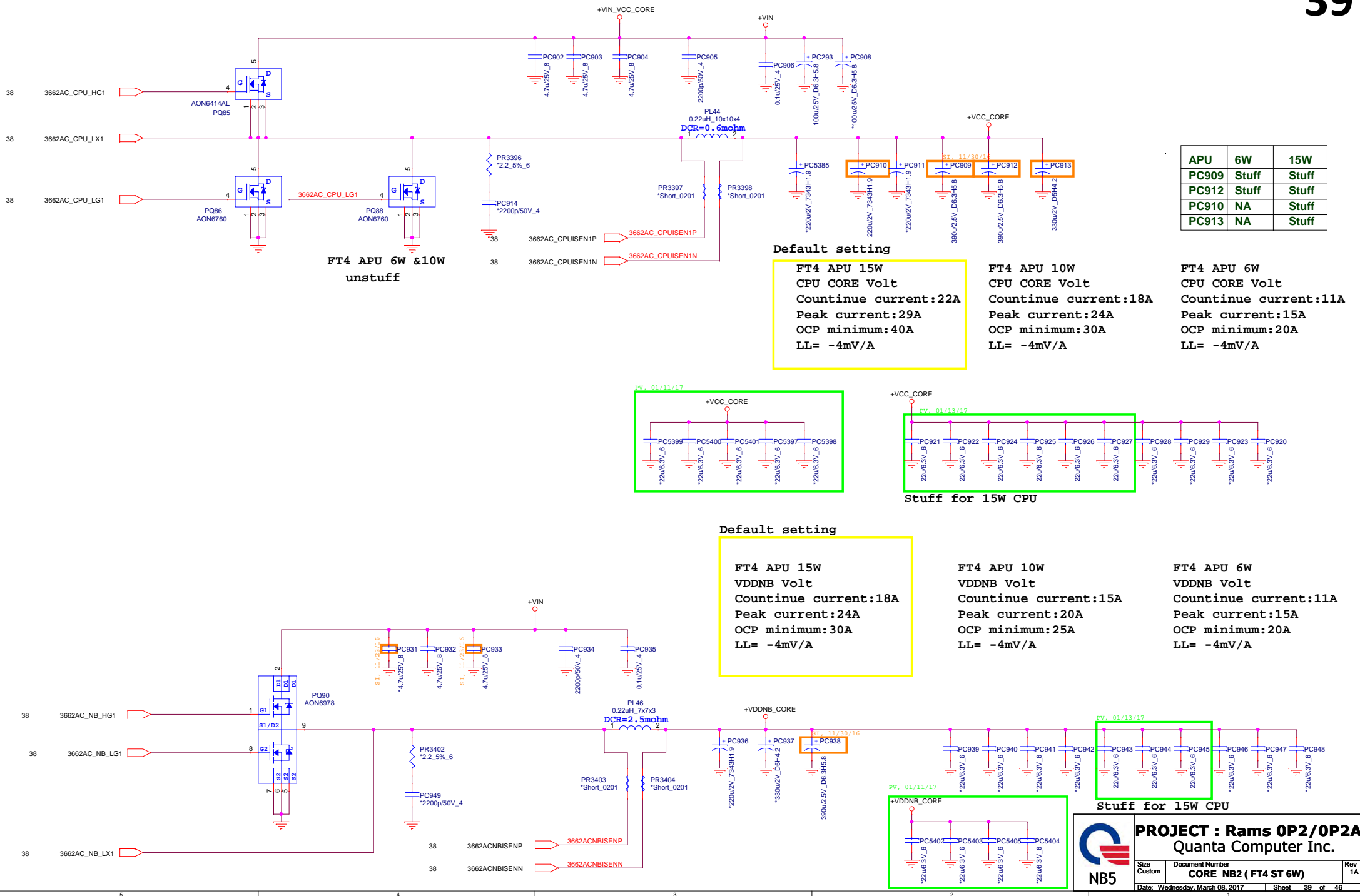



Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k

	R1		
Stoney / Bristol	1.91K	CS21912FB13	0.95V
	3.16K	CS23162FB04	1.05V








 NB5	<b>PROJECT : Rams OP2/OP2A</b> Quanta Computer Inc.		
	Size Custom	Document Number <b>GFX1 ( Stonlry N/A)</b>	Rev 1A
	Date: Wednesday, March 08, 2017      Sheet 40 of 46		



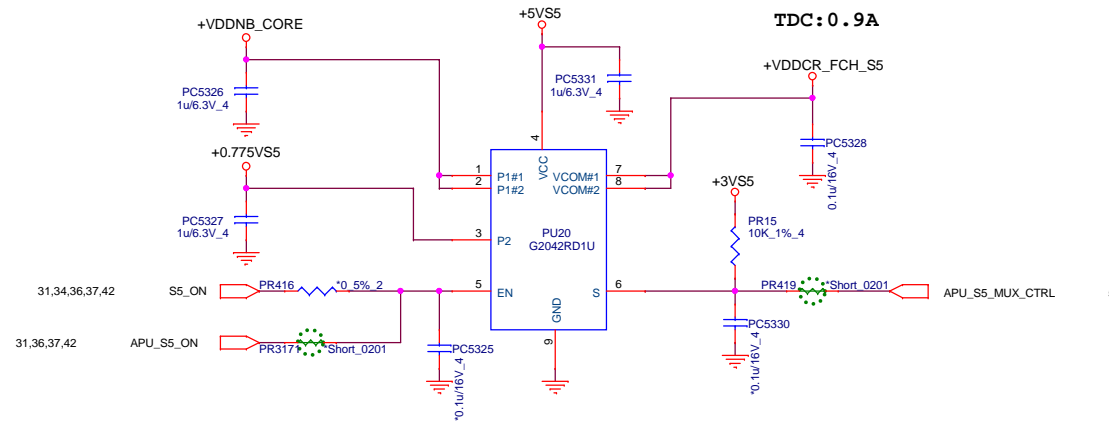
CPU	Page 40 & Page 41
Bristol	Stuff
Stonley FP4,FT4	Unstuff



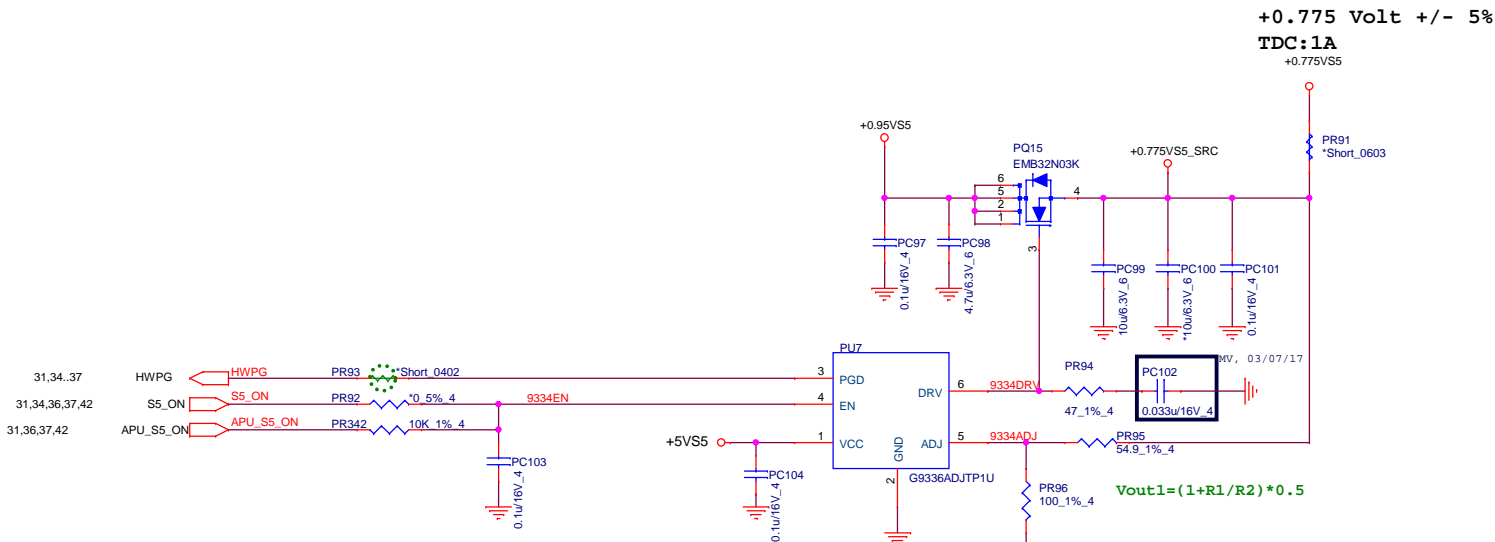
PROJECT : Rams OP2/OP2A

Quanta Computer Inc.

Size Custom	Document Number GFX2 ( Stonlry N/A)	Rev 1A
Date: Wednesday, March 08, 2017		
Sheet 41 of 46		

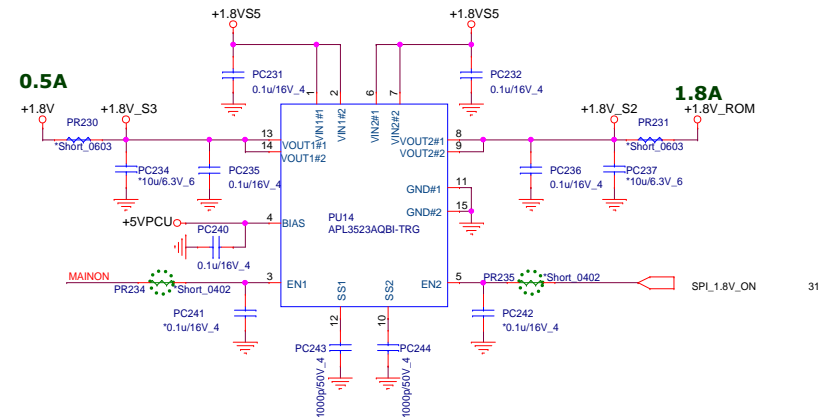
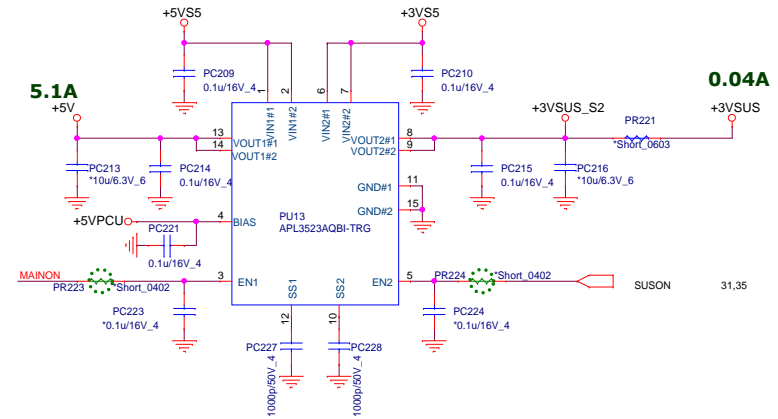


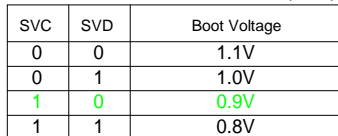
EN	SEL	VIN1	Vo
0	X	0.775V~1.2V	0V
1	0	<0.775V	0.775V
1	0	>0.775V	VDDNB
1	1	0.775V~1.2V	VDDNB



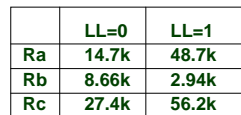
**PROJECT : Rams OP2/OP2A**  
**Quanta Computer Inc.**

Size Custom	Document Number VDDCR_FCH/0.775VS5	Rev 1A
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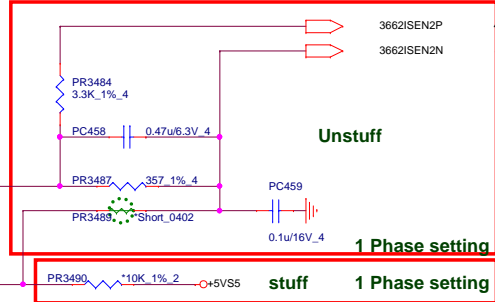




SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V



	LL=0	LL=1
Ra	14.7k	48.7k
Rb	8.66k	2.94k
Rc	27.4k	56.2k

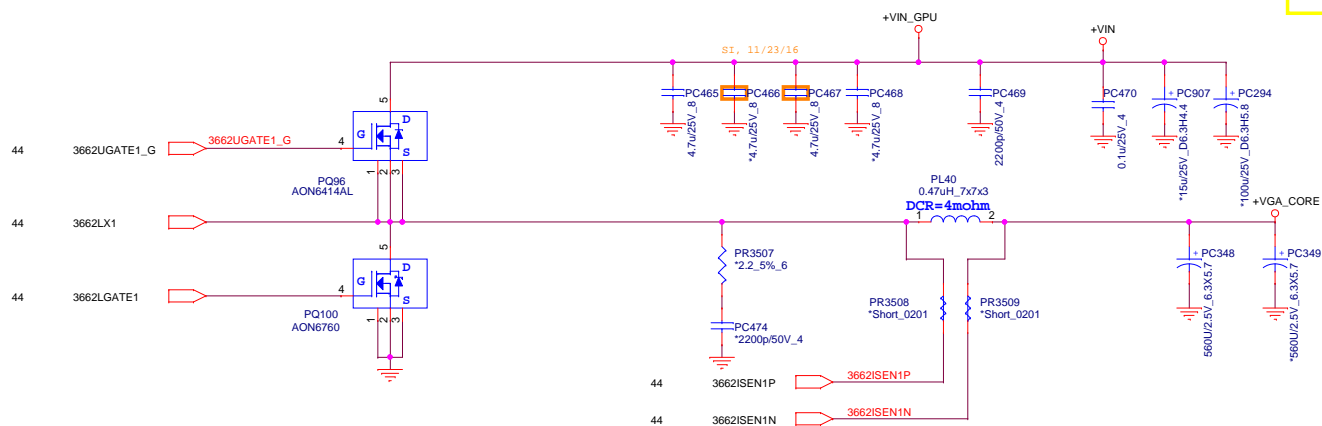


	1 Phase setting	
R1		
R2		
R3		

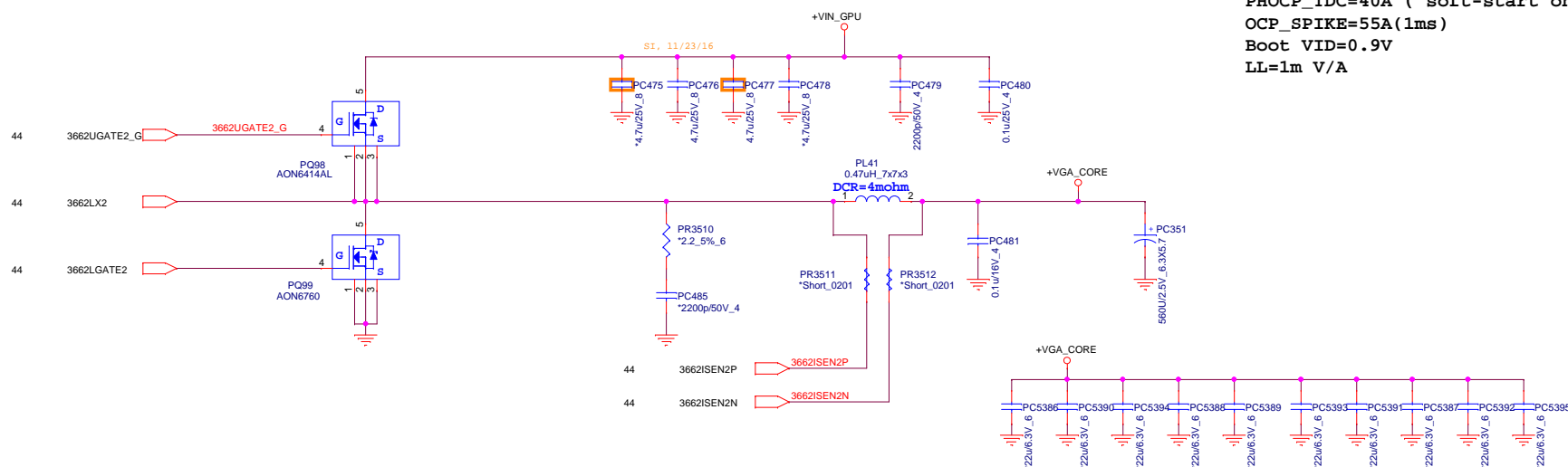
	1 Phase setting	
R1		
R2		
R3		

	1 Phase setting	
R4		

Default M1-30  
 VGACORE ( R17M-M1-30\_18W/25W(1ms) )  
**Countinue current:28A**  
 Peak current=38A (1ms)  
 PHOCP\_TDC=40A ( soft-start only)  
 OCP\_SPIKE=55A(1ms)  
 Boot VID=0.9V  
 LL=0m V/A



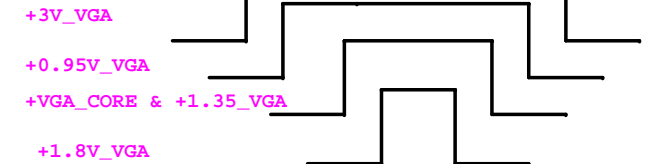
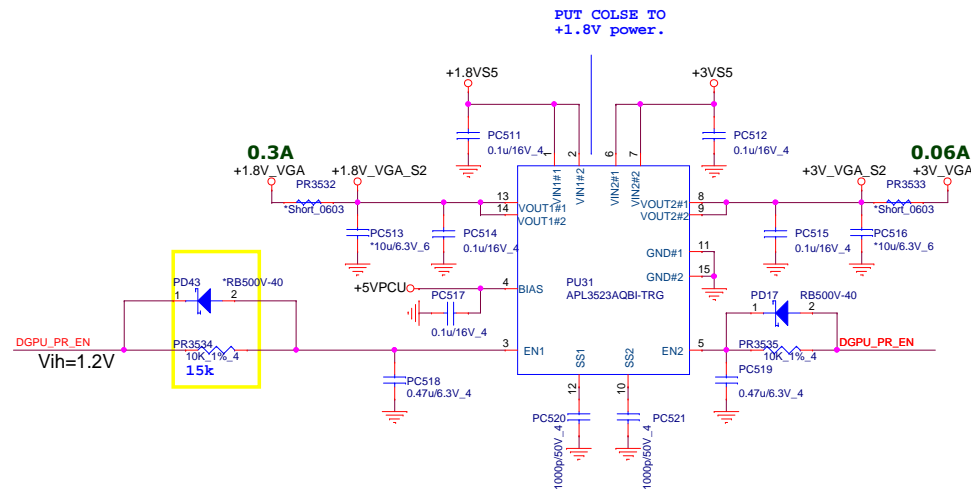
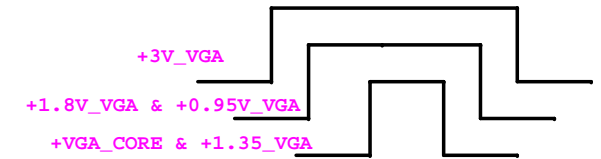
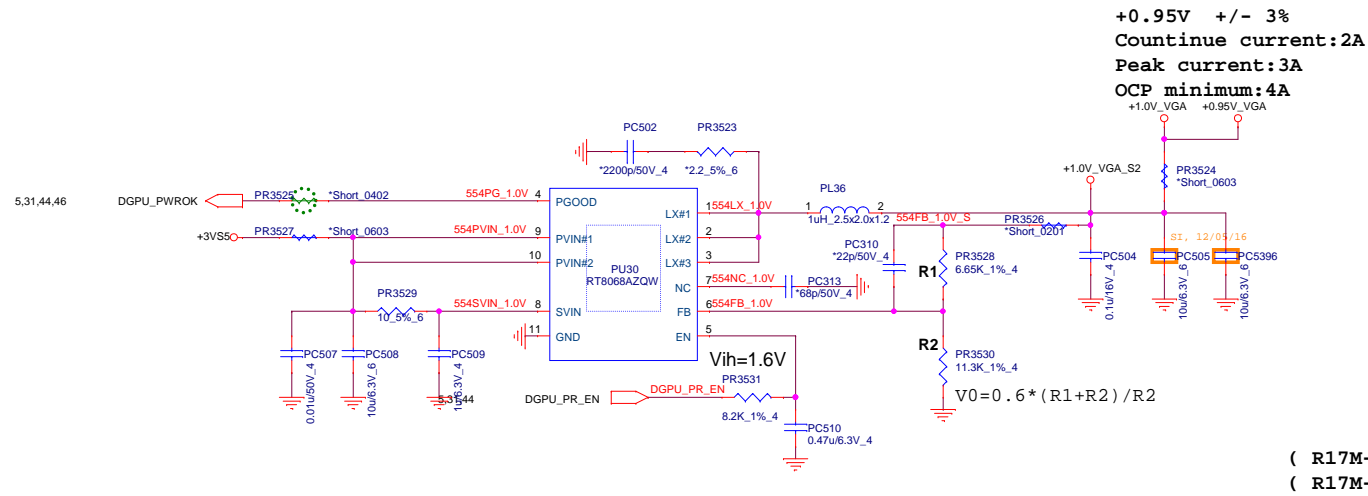
VGACORE ( R17M-M1-70\_25W/38W(1ms) )  
**Countinue current:28A**  
 Peak current=38A (1ms)  
 PHOCP\_TDC=40A ( soft-start only)  
 OCP\_SPIKE=55A(1ms)  
 Boot VID=0.9V  
 LL=1m V/A






**R**

A



 NB5	<b>PROJECT : Rams OP2/OP2A</b> Quanta Computer Inc.				
	Size Custom	Document Number <b>Storage Mode/NA</b>			Rev 1A
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